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LCD Monitor

Service Manual

MODEL:
LCT-17HT

CONTENTS

SPECIFICATION

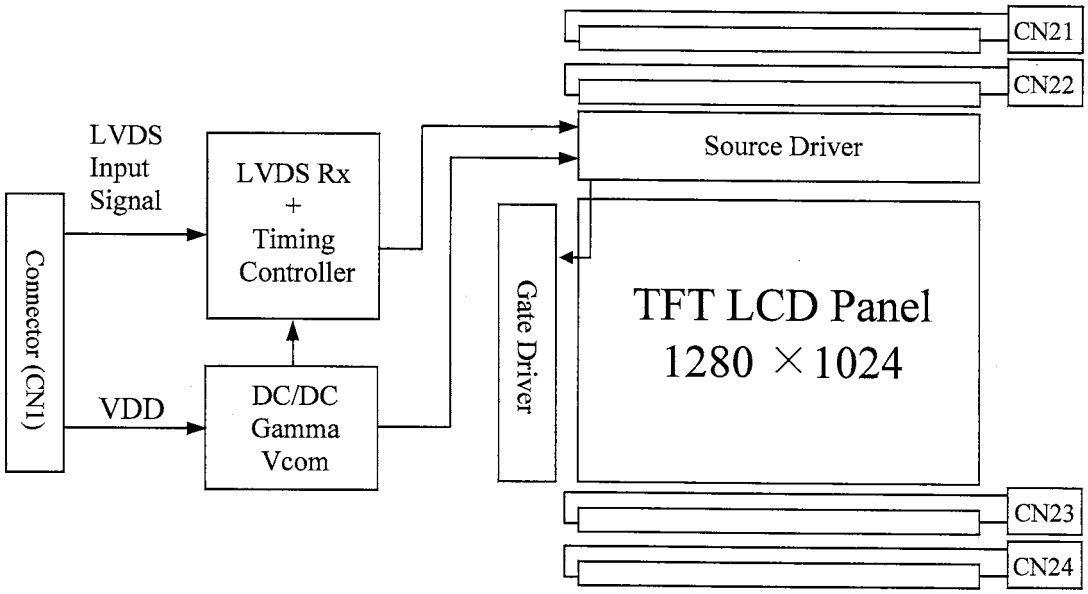
- Resolution: 17.0 inch SXGA (1280 x 1024 @75Hz)
- Color display: 16,777,216 colors
- DPMS (Display Power Management Signaling)
- OSD (On Screen Display)
- Auto Configuration: Hot Key
- Speaker [L + R: 3W + 3W = 6W (max)]
- DDC 1/2 B: Plug & Play

PANEL: HT17E12-200

1. GENERAL DESCRIPTION

1.1 Introduction

HT17E12-200 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 17.0 inch diagonally measured active area with SXGA resolutions (1280 horizontal by 1024 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16,194,227 colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- LVDS Interface with 2 pixel / clock
- High-speed response
- Low power consumption
- 6-bit (FRC) color depth, display 16,194,227 colors
- Incorporated edge type back-light (Four lamps)
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) mode

1.3 Applications

- Desktop Type of PC & Workstation Use
- Slim-Size Display for Stand-alone Monitor
- Display Terminals for Control System
- Monitors for Process Controller

1.4 General Specifications

The followings are general specifications at the model HT17E12-200

<Table 1. General Specifications>

Parameter	Specification	Unit
Active area	337.92 (H) × 270.336(V)	Mm
Number of pixels	1280(H) × 1024(V)	pixels
Pixel pitch	0.264(H) × 0.264(V)	Mm
Pixel arrangement	RGB Vertical stripe	
Display colors	16,194,227	colors
Display mode	Normally White	
Dimensional outline	358.5(H) × 296.5(V) × 17.0(D) type	Mm
Weight	1900 max.	gram
Back-light	Top/Bottom edge side 4-CCFL type	

Note: 1. CCFL (Cold Cathode Fluorescent Lamp)

2.0 ABSOLUTE MAXIMUM RATINGS

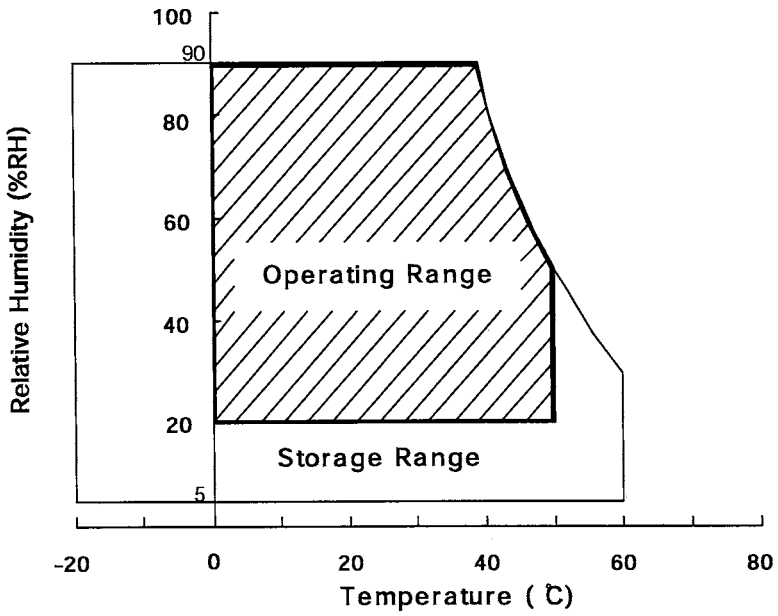
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

<Table 2. Absolute Maximum Ratings> [VSS = GND =0V]

Parameter	Symbol	Min	Max	Unit	Remarks
Power Input Voltage	V_{DD}	VSS-0.5	6.5	V	Ta=25°C
Logic Input Voltage	V_{IN}	VSS-0.3	V_{DD}+0.3	V	
Back-light Lamp Current	I_{BL}	3	7	mA	
Back-light lamp Frequency	F_L	30	(80)	KHz	
Operating Temperature	T_{OP}	0	+50	°C	1)
Storage Temperature	T_{ST}	-20	+60	°C	1)

Notes:

1. Temperature and relative humidity range are shown in the figure below.
2. Wet bulb temperature should be 39°C max and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

< Table 3. Electrical specifications > [Ta = 25±2°C]

Parameter		Min	Typ	Max	Unit	Remarks
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V	Note1
Power Supply Current	I_{DD}	-	580	700	mA	
Permissible Input Ripple Voltage	V_{RF}			100	mV	V_{DD} = 5.0V
High Level Differential Input Threshold Voltage	V_{IH}		-	+100	mV	Vcm = 1.2V typ
Low Level Differential Input Threshold Voltage	V_{IL}	-100	-		mV	
Back-light Lamp Voltage	V_{BL}	690	700	840	V_{rms}	
Back-light Lamp Current	I_{BL}	3.0	6.5	7.0	mA_{rms}	
Back-light Lamp operating Frequency	F_L	30	-	70	KHz	Note 2
Lamp Start Voltage			940	1170	V_{rms}	25°C, Note 3
			1340	1570	V_{rms}	0°C, Note 3
Lamp Life		40000	50000		hrs	I_{BL} = 6.5mA
Power Consumption	P_D		2.9		W	I_{BL}= 6.5mA, Note 4
	P_{BL}		18.2		W	
	P_{total}		21.1		W	

Notes:

1. The supply voltage is measured and specified at the interface connector of LCM. The current draw and power consumption specified is for VDD = 5.0V, Frame rate= 75Hz and Clock frequency = 67.5MHz. Test Pattern of power supply current
    a. Typ: Black pattern
    b. Max: Dot pattern
2. The lamp frequency should be selected as different as possible from the horizontal synchronous frequency and its harmonics to avoid interference, which may cause line flow on the display
3. The voltage above this value should be applied to the lamps for more than 1 second to start-up. Otherwise the lamps may not be turned on.
4. Calculated value for reference (V_{BL} × I_{BL}) × 4 excluding inverter loss.

4.0 OPTICAL SPECIFICATIONS

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and φ equal to 0°. We refer to θφ=0 (=θ3) as the 3 o'clock direction (the "right"), θφ=90 (=θ12) as the 12 o'clock direction ("upward"), θφ=180 (=θ9) as the 9 o'clock direction ("left") and θφ=270 (=θ6) as the 6 o'clock direction ("bottom"). While scanning θ and/or φ, the center of the measuring spot on the display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 5.0V +/- 10% at 25°C. Optimum viewing angle direction is 6 o'clock.

4.2 Optical Specifications

[VDD=5.0V, Frame rate=60Hz, Clock=54MHz, IBL = 6.5mA, Ta = 25±2℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR>10	75	80	-	Deg	Note 1
		Θ_9		75	80	-	Deg	
	Vertical	Θ_{12}		60	65	-	Deg	
		Θ_6		60	65	-	Deg	
	Horizontal	Θ_3	CR>5	80	85	-	Deg	
		Θ_9		80	85	-	Deg	
	Vertical	Θ_{12}		70	75	-	Deg	
		Θ_6		70	75	-	Deg	
Luminance contrast ratio		CR	$\Theta=0^o$ (Center) Normal Viewing Angle	350	430	-		Note 2
Luminance of white		Y_W		200	250	-	cd/m^2	Note 3
White luminance uniformity		ΔY		-	-	1.2		Note 4
Reproduction of color	White	Wx		0.270	0.300	0.330		Note 5
		Wy		0.305	0.335	0.365		
	Red	Rx		0.599	0.629	0.659		
		Ry		0.324	0.354	0.384		
	Green	Gx		0.257	0.287	0.317		
		Gy		0.568	0.598	0.628		
	Blue	Bx		0.115	0.145	0.175		
		By		0.073	0.103	0.133		
Response time		Tr		-	5	30	msec	Note 6
		Td		-	15			
Cross talk		CT		-	-	2.0	%	Note 7

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

   $$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Maximum Luminance of five points / Minimum Luminance of five points (See FIGURE 2 shown in appendix).
5. The color chromaticity coordinates specified in Table 4. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as FIGURE 3 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td, and 90% to 10% is Tr.
7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See FIGURE 4 shown in Appendix).

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

CN11: Module Side Connector : FI-XB30S-HF (JAE) or Equivalent
User Side Connector : FI-X30H-HF (JAE) or equivalent

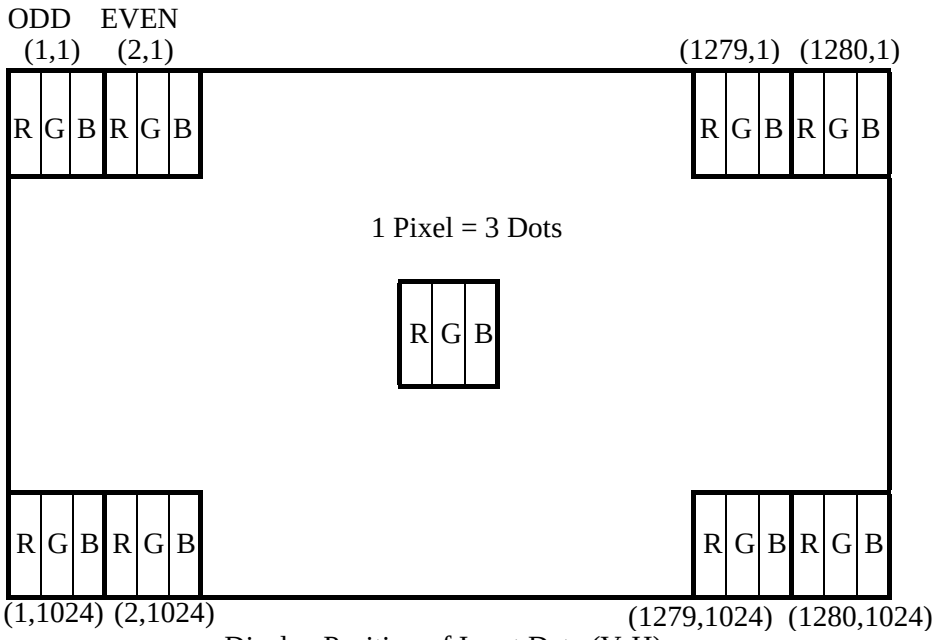
Pin No	Symbol	Function	Remark
1	RXO0-	LVDS ODD 0 – SIGNAL	
2	RXO0+	LVDS ODD 0 + SIGNAL	
3	RXO1-	LVDS ODD 1 – SIGNAL	
4	RXO1+	LVDS ODD 1 + SIGNAL	
5	RXO2-	LVDS ODD 2 – SIGNAL	
6	RXO2+	LVDS ODD 2 + SIGNAL	
7	GND	GROUND	
8	RXOCLK-	LVDS ODD CLOCK – SIGNAL	
9	RXOCLK+	LVDS ODD CLCOK + SIGNAL	
10	RXO3-	LVDS ODD 3 – SIGNAL	
11	RXO3+	LVDS ODD 3 + SIGNAL	
12	RXE0-	LVDS EVEN 0 – SIGNAL	
13	RXE0+	LVDS EVEN 0 + SIGNAL	
14	GND	GROUND	
15	RXE1-	LVDS EVEN 1 – SIGNAL	
16	RXE1+	LVDS EVEN 1 + SIGNAL	
17	GND	GROUND	
18	RXE2-	LVDS EVEN 2 – SIGNAL	
19	RXE2+	LVDS EVEN 2 + SIGNAL	
20	RXECLK-	LVDS EVEN CLOCK – SIGNAL	
21	RXECLK+	LVDS EVEN CLOCK + SIGNAL	
22	RXE3-	LVDS EVEN 3 – SIGNAL	
23	RXE3+	LVDS EVEN 3 + SIGNAL	
24	GND	GROUND	
25	NC	NO CONECTION	
26	DE	NO CONECTION	
27	NC	NO CONECTION	
28	VDD	POWER SUPPLY (+5.0V)	
29	VDD		
30	VDD		

5.2 LVDS Interface (Tx: THC63LVDF83A or Equivalent)

	Input signal	Transmitter		Interface		FI-X30S-HF	Remark
		Pin No	Pin No	System (Tx)	TFT-LCD (Rx)	Pin No.	
ODD LVDS	OR0	51	48 47	OUT0- OUT0+	RXO0- RXO0+	1 2	
	OR1	52					
	OR2	54					
	OR3	55					
	OR4	56					
	OR5	3					
	OG0	4					
	OG1	6	46 45	OUT1- OUT1+	RXO1- RXO1+	3 4	
	OG2	7					
	OG3	11					
	OG4	12					
	OG5	14					
	OB0	15					
	OB1	19					
	OB2	20	42 41	OUT2- OUT2+	RXO2- RXO2+	5 6	
	OB3	22					
	OB4	23					
	OB5	24					
	HSYNC	27					
	VSYNC	28					
	DE	30					
	MCLK	31	40 39	CLKOUT- CLKOUT+	RXO CLK- RXO CLK+	8 9	
	OR6	50	38 37	OUT3+ OUT3-	RXO3- RXO3+	10 11	
	OR7	2					
	OG6	8					
	OG7	10					
	OB6	16					
	OB7	18					
	RSVD	25					
EVEN LVDS	ER0	51	48 47	OUT0- OUT0+	RXE0- RXE0+	12 13	
	ER1	52					
	ER2	54					
	ER3	55					
	ER4	56					
	ER5	3					
	EG0	4					

	Input signal	Transmitter		Interface		FI-X30S-HF	Remark
		Pin No	Pin No	System (Tx)	TFT-LCD (Rx)	Pin No.	
EVEN LVDS	EG1	6	46 45	OUT1- OUT1+	RXE1- RXE1+	15 16	
	EG2	7					
	EG3	11					
	EG4	12					
	EG5	14					
	EB0	15					
	EB1	19					
	EB2	20	42 41	OUT2 – OUT2+	RXE2- RXE2+	18 19	
	EB3	22					
	EB4	23					
	EB5	24					
	HSYNC	27					
	VSYNC	28					
	DE	30					
	MCLK	31	40	CLKOUT-	RXE CLK-	20	
			39	CLKOUT+	RXE CLK+	21	
	ER6	50	38 37	OUT3+ OUT3 -	RXE3- RXE3+	22 23	
	ER7	2					
	EG6	8					
	EG7	10					
	EB6	16					
	EB7	18					
	RSVD	25					

5.3 Data Input Format



Display Position of Input Data (V-H)

5.4 Back-light Interface Connection

CN21, 22, 23, 24: Module side connector : BHSR-02VS-1 (JST)

User side connector : SM02B-BHSS-1-TB (JST) or equivalent

Pin No	INPUT	Color	Function
1	HOT	Pink & White	High voltage
2	COLD	Black & White	Ground

6.0 SIGNAL TIMING SPECIFICATION

6.1 The HT17E12-200 is operated by the only DE (Data enable) mode (LVDS Transmitter Input)

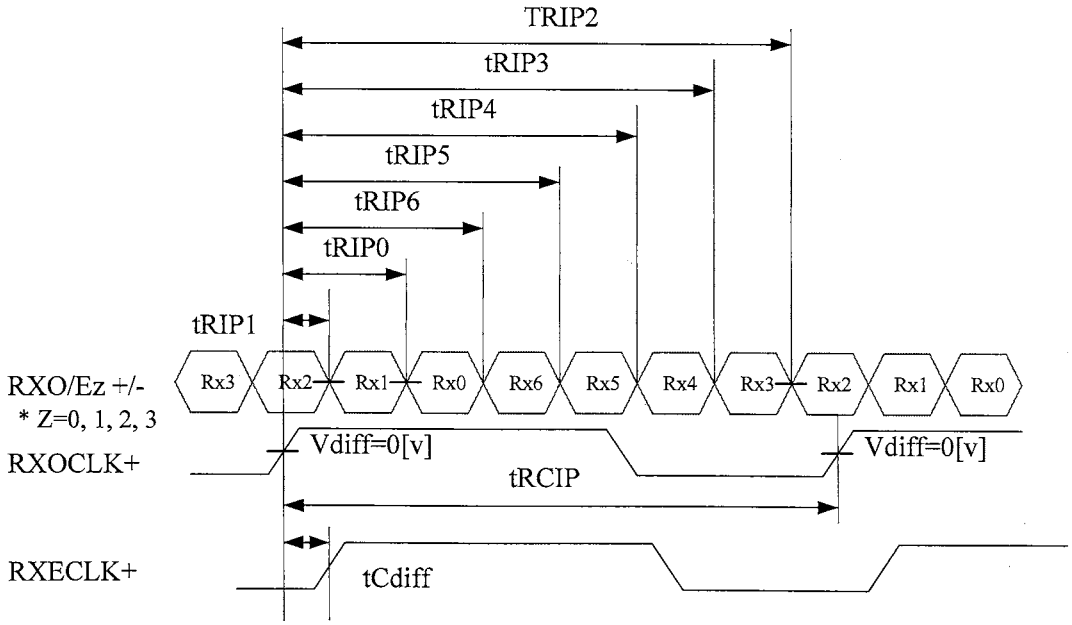
Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	40	54	68	MHz
	High Time	Tch	5	-	-	ns
	Low Time	Tcl	5	-	-	ns
Data	Setup Time	Tds	4	-	-	ns
	Hold Time	Tdh	4	-	-	ns
Data Enable Setup Time		Tes	4	-	-	ns
Frame Period		Tv	1032	1066	1536	lines
			13.33	16.67	-	msec
Vertical Display Period		Tvd	-	1024	-	lines
One Line Scanning Period		Th	672	844	1022	clocks
Horizontal Display Period		Thd	640	640	640	clocks

6.2 LVDS Rx interface timing parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 4.

< Table 4. LVDS Rx Interface Timing Specification>

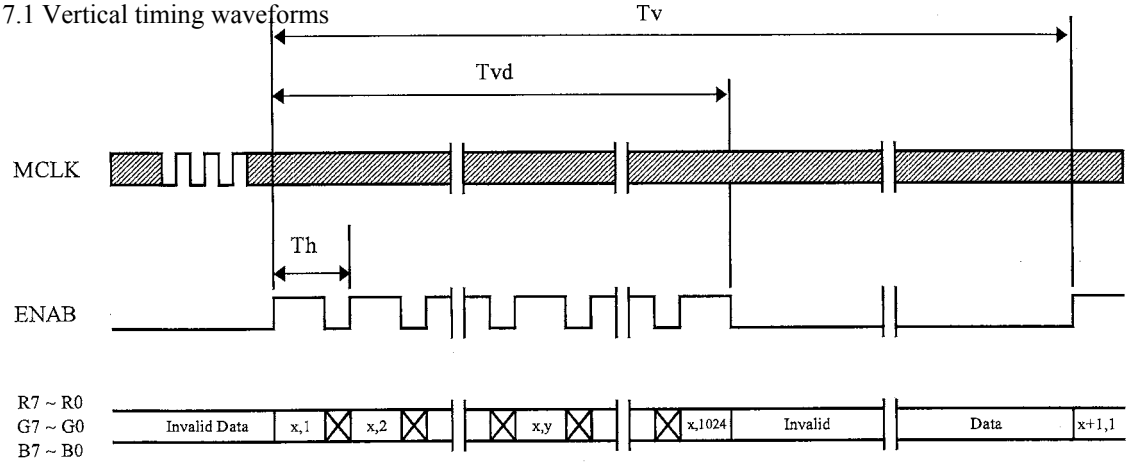
Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCIP	14.7	18.5	-	nsec	
CLK Difference	tCdiff	-tRCIP*(3/7)	0	+tRCIP*(3/7)	nsec	
Input Data 0	tRIP1	-0.4	0	+0.4	nsec	
Input Data 1	tRIP0	1*tRICP/7-0.4	1*tRICP/7	1*tRICP/7+0.4	nsec	
Input Data 2	tRIP6	2*tRICP/7-0.4	2*tRICP/7	2*tRICP/7+0.4	nsec	
Input Data 3	tRIP5	3*tRICP/7-0.4	3*tRICP/7	3*tRICP/7+0.4	nsec	
Input Data 4	tRIP4	4*tRICP/7-0.4	4*tRICP/7	4*tRICP/7+0.4	nsec	
Input Data 5	tRIP3	5*tRICP/7-0.4	5*tRICP/7	5*tRICP/7+0.4	nsec	
Input Data 6	tRIP2	6*tRICP/7-0.4	6*tRICP/7	6*tRICP/7+0.4	nsec	



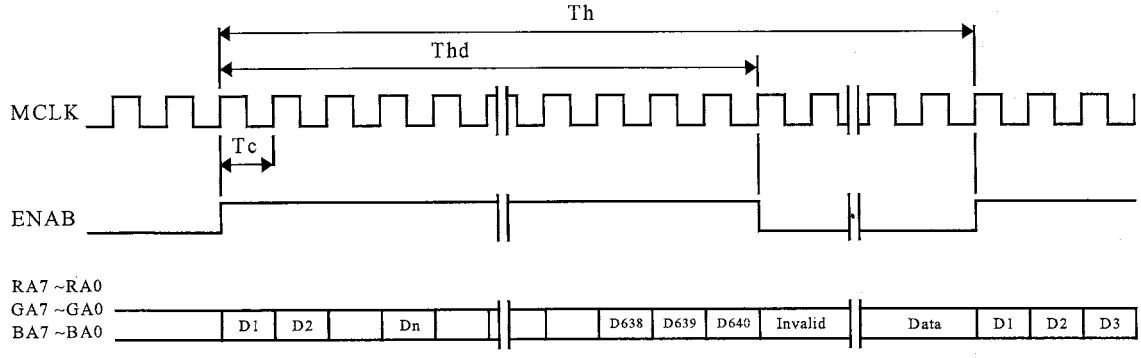
* Vdiff = (RXO/Ez+)-(RXO/Ez-), ….. , (RXO/ECLK+)-(RXO/ECLK-)

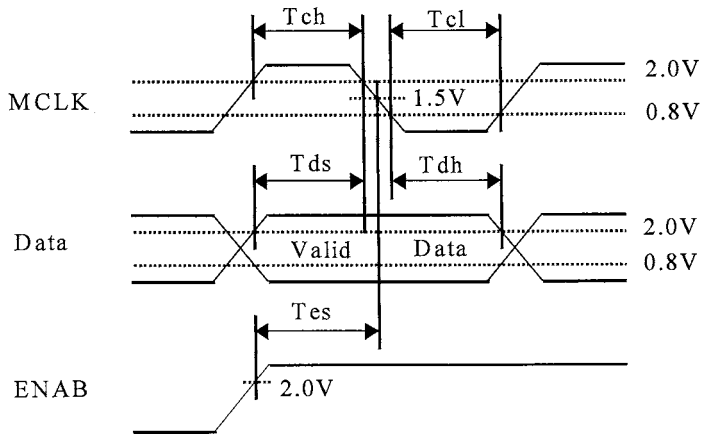
7.0 SIGNAL TIMING WAVEFORMS OF INTERFACE SIGNAL

7.1 Vertical timing waveforms



7.2 Horizontal Timing Waveforms



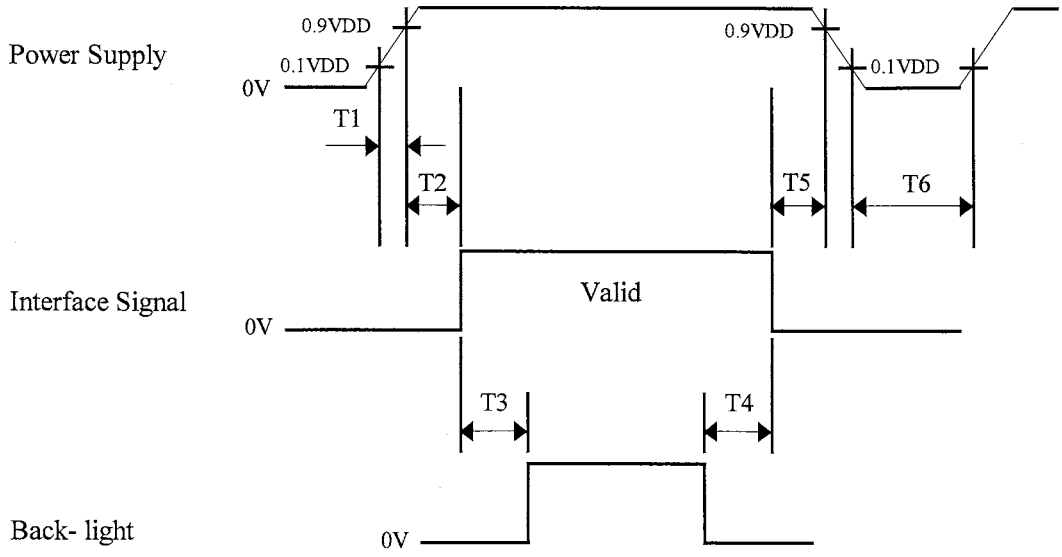


8.0 INPUT SIGNAL, BASIC DISPLAY COLORS & GRAY SCALE OF COLOR

Colors & Gray Scale		Red data								Green data								Blue data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▲	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▲ ▼	↑ ↓								↑ ↓								↑ ↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▼	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▲	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	▲ ▼	↑ ↓								↑ ↓								↑ ↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▼	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▲	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	▲ ▼	↑ ↓								↑ ↓								↑ ↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▼	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale Of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▲	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	▲ ▼	↑ ↓								↑ ↓								↑ ↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▼	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as shown in below.



- 0 < T1 ≤ 10 ms
- 20ms < T2 ≤ 50 ms
- 500 ms ≤ T3
- 100 ms ≤ T4
- 0 < T5 ≤ 50 ms
- 1 sec ≤ T6

Notes:

1. When the power supply VDD is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

10.0 MECHANICAL CHARACTERSTICS

10.1 Dimensional Requirement

FIGURE 6 shown in appendix shows mechanical outlines for the model HT17E12-200. Other parameter are shown in Table 5.

<Table 5. Dimensional Parameter>

Parameter	Specification	Unit
Dimensional outline		
Horizontal	358.5 ± 0.5	Mm
Vertical	296.5 ± 0.5	
Thickness	17.0 ± 0.5	
Weight	1900 max	Gram
Active area	337.92 (h) x 270.336 (v)	Mm
Pixel pitch	0.264 (h) x 0.264 (v)	Mm
Number of pixels	1280 (h) x 1024 (v) (1 pixel = R + G + B dot)	Pixels
Back-light	Top/bottom edge 4-CCFL type	

10.2 Mounting

See FIGURE 5 shown in appendix

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50[cm] from the screen with an overhead light level of 350[lux].

The manufacture shall furnish limit samples of the panel showing the lightest leakage acceptable.

11.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 6. Reliability Test Parameter>

No	Test Items	Conditions	
1	High temperature storage test	Ta = 60°C, 240 hrs	
2	Low temperature storage test	Ta = -20°C, 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C, 80 %RH, 240 hrs	
4	High temperature operation test	Ta = 50°C, 240 hrs	
5	Low temperature operation test	Ta = 0°C, 240 hrs	
6	Thermal shock	Ta = -20°C ↔ 60°C (30 min), 100 cycle	
7	Vibration test (non-operating)	Frequency	: 10 ~ 300 Hz, Sweep rate 30min
		Gravity/AMP	: 1.5G
		Period	: ±X, ±Y, ±Z 30min
8	Shock test (non-operating)	Gravity	: 70G
		Pulse width	: 11ms, sine wave
			± X, ± Y, ± Z Once for each direction
9	Electrostatic discharge test	Air	: 150 pF, 330Ω, 15KV
		Contact	: 150 pF, 330Ω, 8KV

12.0 HANDLING & CAUTIONS

12.1 Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

12.2 Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back-light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry-cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

12.3 Cautions for the operation

- When the module is operating, do not lose LVDS signals. If any one of these signals were lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If the wrong sequences were applied, the module would be damaged.

12.4 Cautions for the atmosphere

- Dewdrop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer-packing pouch and under relatively low temperature atmosphere is recommended.

12.5 Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at aging time.
- Applying fixed pattern for a long time may cause image sticking.

12.6 Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc, please pack the module not to be broken. We recommend on using the original shipping packages.

14.0 APPENDIX

Figure 1. Measurement Set Up

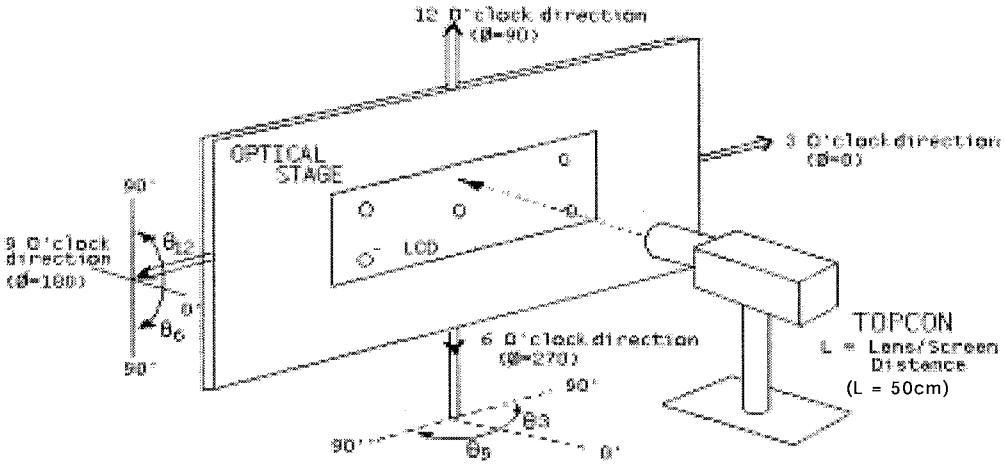


Figure 2. Average Luminance Measurement Locations & Uniformity Measurement Locations.

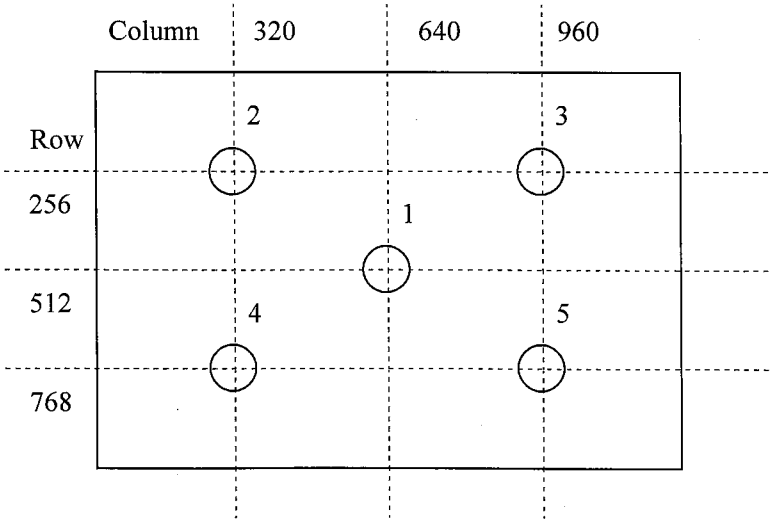


Figure 3. Response Time Testing

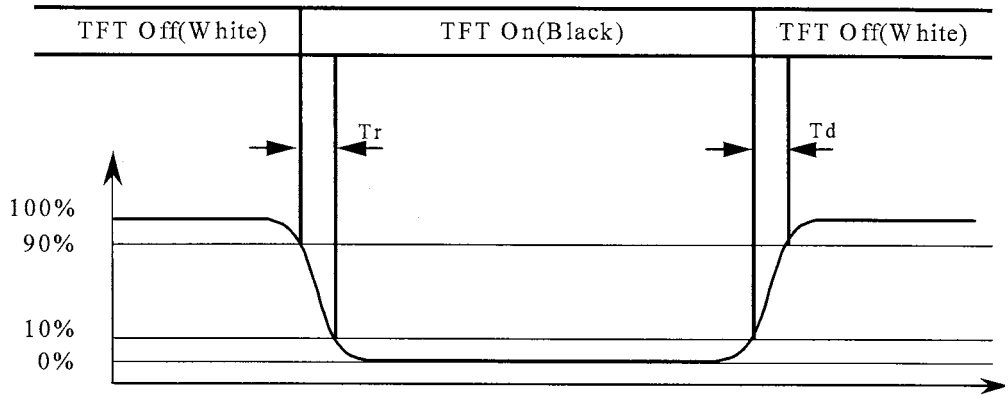
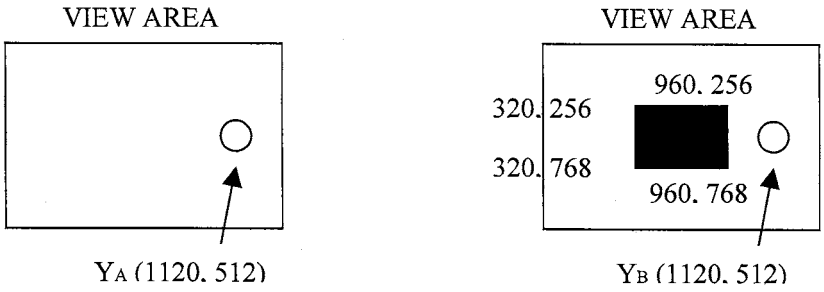


Figure 4. Cross Modulation Test Description



$$\text{Cross-Talk} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns.

Figure 5. TFT-LCD Module Outline Dimensions (Front View)

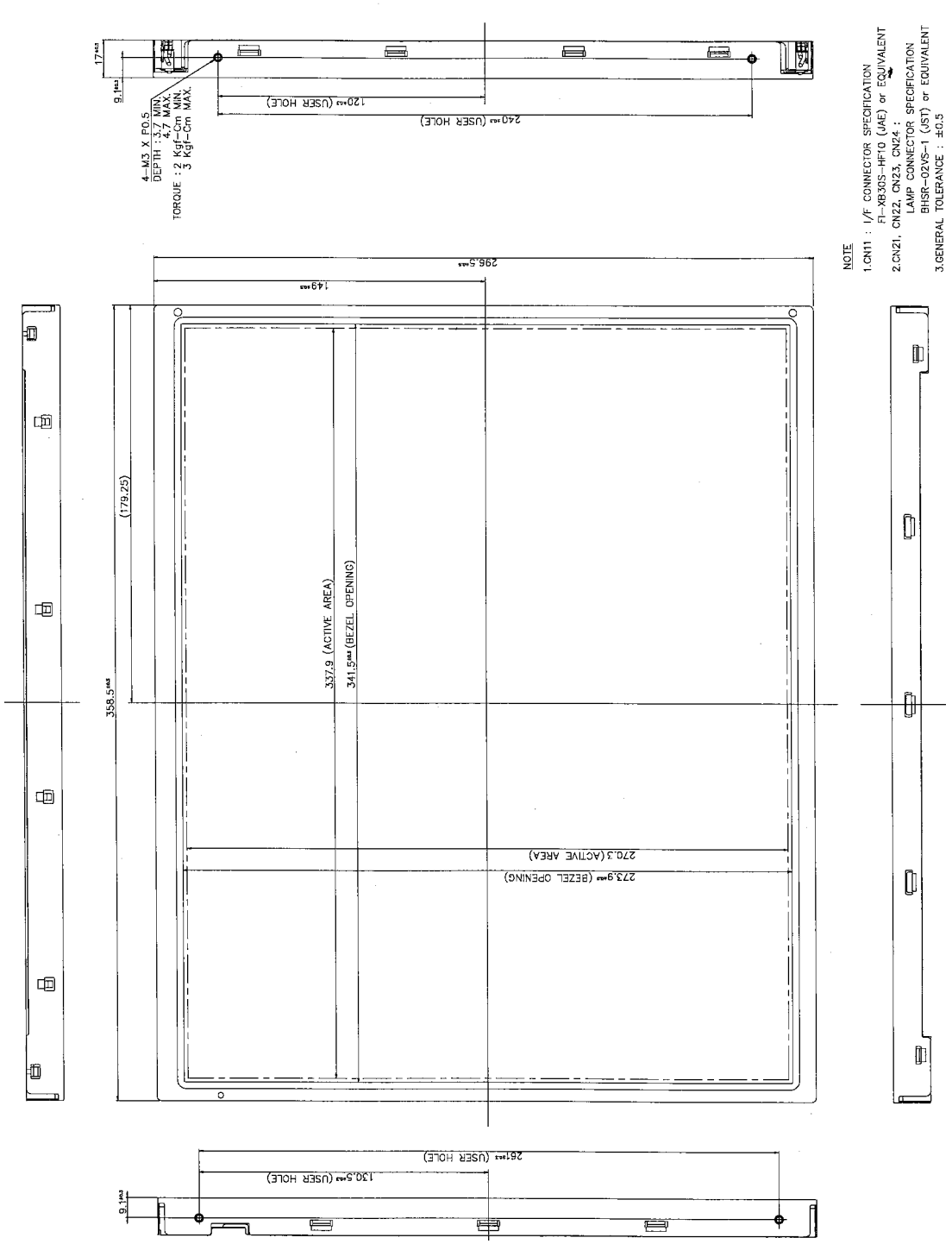
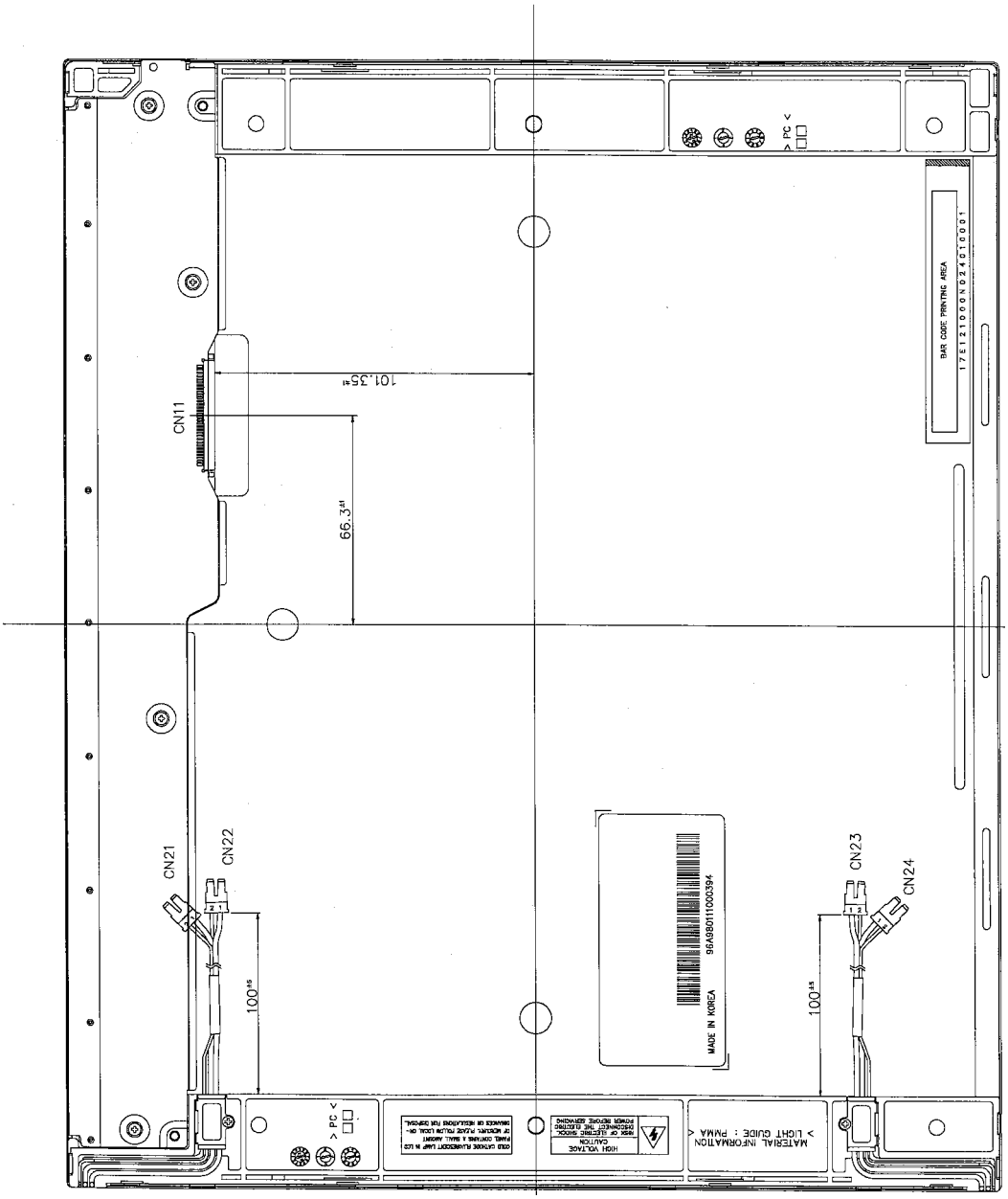


Figure 6. TFT-LCD Module Outline Dimensions (Rear view)



8 BIT MTP MICROCONTROLLER

1.0 FEATURES

- 8051 instruction set compatible 8-bit microcontroller
- 8051/8052 compatible pinout
- Complete static design, wide range of operation frequency from 1 ~ 40 MHz
- Large on-chip memory
  - 64K bytes built-in Multiple Times Programmable ROM (MTP-ROM) program memory
  - 512 bytes on-chip SRAM, expandable external 64K bytes address space
- Dual Data Pointer
- Four 8-bit bi-directional I/O ports
- 6 interrupts including 2 external sources
- One full-duplex serial UART ports compatible with standard 8052
- Three 16 bit timer/counters
- On chip oscillator for crystal
- Software Power-Down mode, supports Idle mode and Power Down mode for less power consumption
- ROM Code Protection
- 4.5V~5.5V operation voltage, 12V programming voltage
- 44-pin PLCC or QFP package

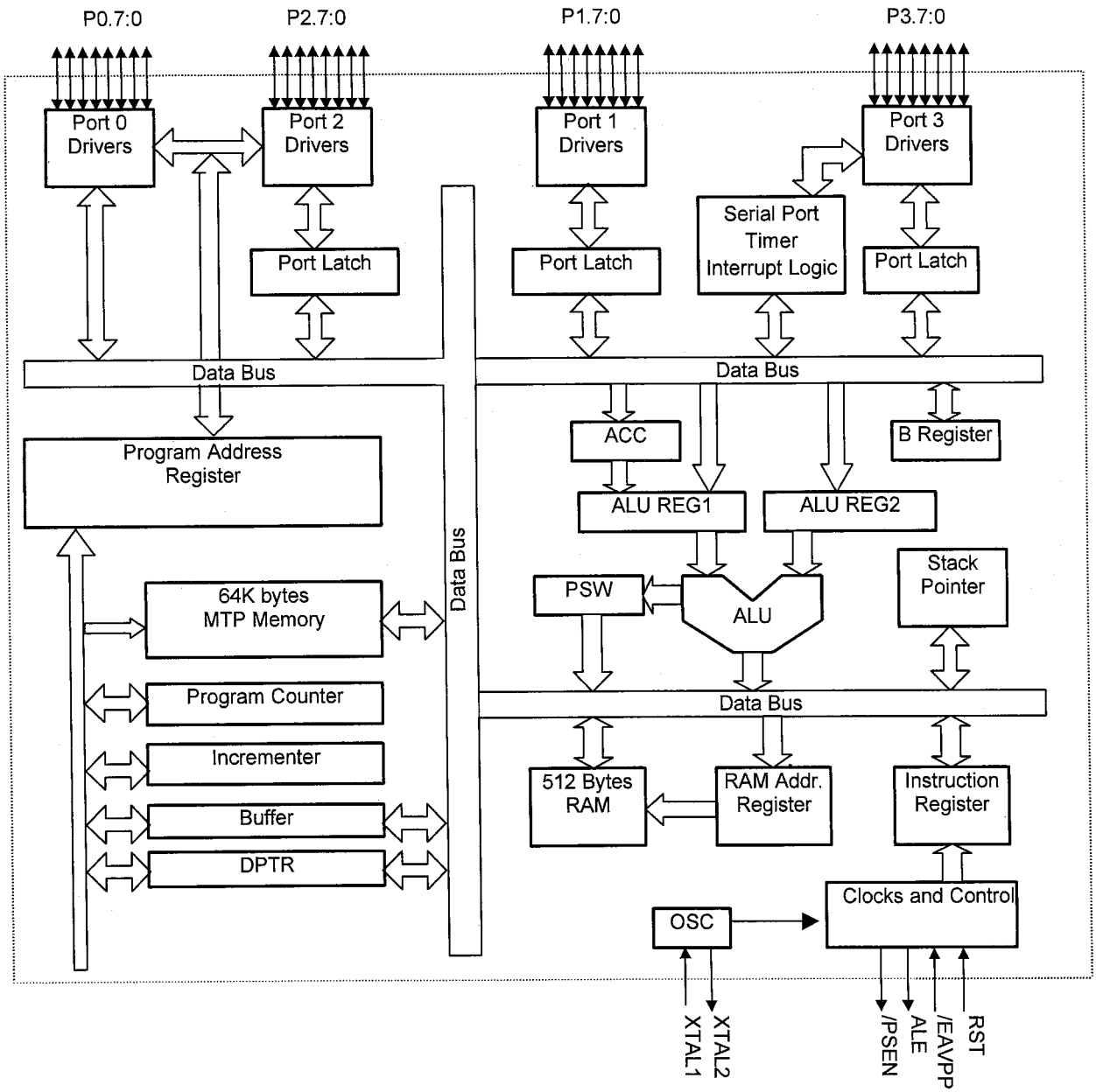
1.1 General Description

The M6759 is an 8032/8052 instruction compatible 8-bit microcontroller with MTP Flash ROM for firmware updating. By combining a versatile 8-bit CPU with MTP-Flash, this device provides whole microcontroller system on one chip and still remains the feasibility for general control systems in a variety of applications. Furthermore, user-defined security registers can protect the firmware after the code is ready.

The M6759 contains the following:

a. A non-volatile 64K bytes Multiple Times Programmable ROMprogram memory.
b. A volatile 512 bytes read/write data memory
c. Four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51)
d. A 16-bit timer (identical to the Timer 2 of the 8052).
e. A multi-source two-priority-level nested interrupt structure.
f. One serial interface (UART) and
g. An on-chip oscillator.

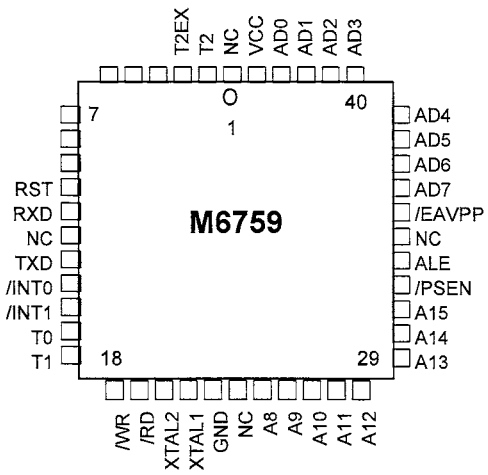
1.2 Block Diagram

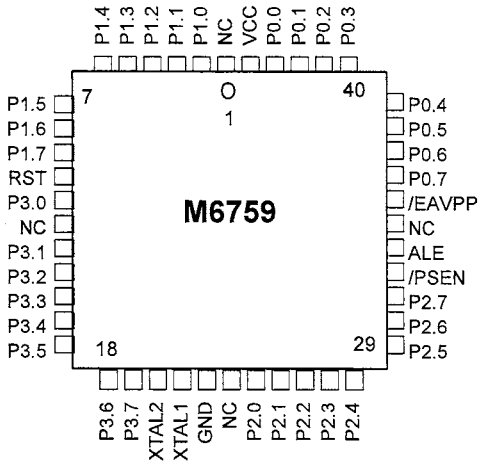


2.0 PIN Description

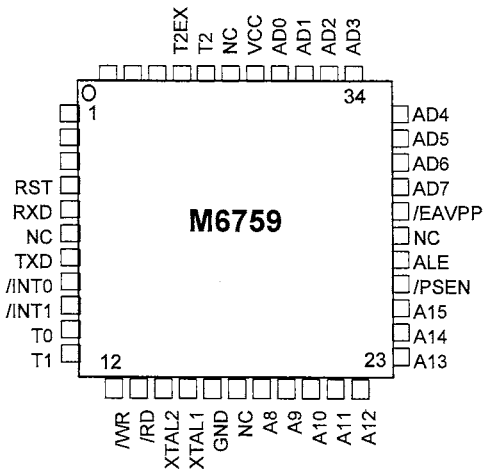
2.1 Pinout Diagram

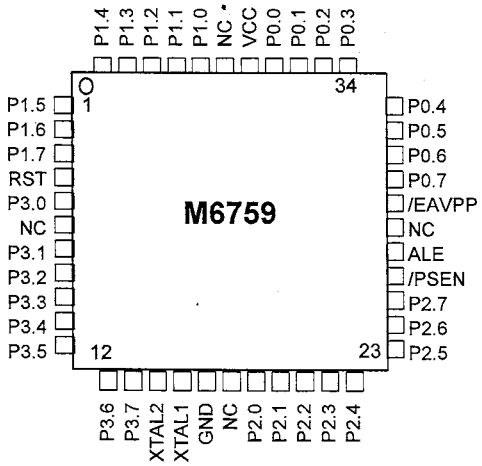
44-pin PLCC Package





44-pin QFP Package





2.2 Pin Description Table

Pin assignments shown below are listed based on 44-pin PLCC package. And if not additionally specified, further pin number reference throughout this datasheet is, by default, referred to 44-pin PLCC package. As for the QFP package, the pin number assignment should be shifted accordingly, as comparatively shown in Section 2.1 Pinout Diagram.

Pin Name	No. (PLCC)	Type	Description
VDD	44	IN	Power supply for internal operation, 5V input.
GND	22	IN	Ground.
P0.7-P0.0 AD7-0	36,37,38,39, 40,41,42, 43	I/O	Port 0 is 8 bits bi-directional I/O port with internal pull high. Multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bi-directional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals.
RST	10	IN	Reset signal of internal circuit, it must be kept 4 clocks to ensure being recognized by internal circuit. This signal will not affect internal SRAM.
XTAL1	21	IN	Crystal In, can be used as external clock input.
XTAL2	20	OUT	Crystal out, feedback of XTAL1.
/PSEN	32	OUT	Program Store Enable Output, commonly connected to external ROM memory as a chip enable during fetching and MOVC operation. /PSEN goes high during a reset condition.
ALE	33	OUT	Address Latch Enable, used to latch external LSB 8 bit address bus from multiplexed address/data bus, commonly connect to the latch enable of 373 family. This signal will be forced high when the device is in a reset condition.
P1.7-P1.0 T2EX (P1.1) T2 (P1.0)	9,8,7,6,5,4,3 ,2	I/O IN IN	Port 1 is 8 bits bi-directional I/O port with internal pull high. All pins have an alternate function shown as below. External timer/counter 2 trigger. External timer/counter 2.
P2.7-P2.0 A15-A8	31,30,29,28, 27,26,25, 24	I/O OUT	Port 2 is 8 bits bi-directional I/O port with internal pull high. The alternate function is MSB 8 bit address bus This bus emits the high-order address byte during fetches from external Program Memory or during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

P3.7-P3.0 /RD (P3.7) /WR (P3.6) T1 (P3.5) T0 (P3.4) /INT1 (P3.3) /INT0 (P3.2) TXD (P3.1) RXD (P3.0)	19,18,17,16, 15,14,13, 11	I/O	Port 3 is an 8-bit bi-directional I/O port with internal pull high. The reset condition of this port is with all bits at a logic 1. Port 3 also have alternate function list below
		OUT	External data memory read strobe.
		OUT	External data memory write strobe.
		IN	External timer/counter 1.
		IN	External timer/counter 0.
		IN	External interrupt 1 (Negative Edge Detect).
		IN	External interrupt 0 (Negative Edge Detect).
		OUT	Serial port output.
		IN	Serial port input.
/EAVPP	35	IN	The pin must be externally held low to enable the device to fetch code from external program memory. If /EAVPP is held high, the device executes from internal program memory. /EAVPP is internal latched on reset. This pin also receives the 12V programming voltage (V_{PP}) during FLASH programming.
NC	1,12,23,34	NC	These pins should not be connected for any purpose

3.0 FUNCTION DESCRIPTION

3.1 Data Space Addressing

The M6759 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes auxiliary RAM (ARAM).

The four segments are:

a. The Lower 128 bytes of RAM (address 00H to 7FH) are directly and indirectly addressable.
b. The Upper 128 bytes of RAM (address 80H to FFH) are indirectly addressable only.
c. The Special Function Registers SFRs, (address 80H to FFH) are directly addressable only.
d. The 256-bytes auxiliary RAM (ARAM, 0000H-00FFH) are indirectly accessed by move external instruction, MOVX.

Either direct or indirect addressing can access the lower 128 bytes. The upper 128 bytes can be accessed by indirect address only. The upper 128 bytes occupy the same address space as the SFRs. That means they have the same address, but are physically separate from SFR space.

The ARAM can be accessed by indirect addressing and MOVX instructions when ARAM_EN bit is set. This part of memory is physically located on-chip, logically occupied the first 256-bytes of external data memory if ARAM_EN bit is set.

The ARAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ARAM will not affect ports P0, P3.6 (/WR) and P3.7 /RD).

If ARAM_EN is cleared, the access to external memory will be performed in the same way as standard 8051. If ARAM_EN is set and DPTR contains value lower than 0100H, the ARAM will be accessed rather than external memory, but if DPTR contains value higher than 00FFH (i.e. 0100H to FFFFH), the external memory will be accessed.

If ARAM_EN is set and P2 SFR contains 00H, the ARAM will be accessed by the MOVX @Ri, #data instruction, but if P2 SFR contains a non-zero value, the external memory will be accessed using MOVX @Ri, #data.

For example,

```
MOVX        DPTR, #data
```

If ARAM_EN is set and DPTR contains 0030H, access the ARAM at address 030H rather than external memory.

If ARAM_EN is set and DPTR contains 0130H, the external memory address 0130H will be accessed

For example:

MOVX @R0, #data

If ARAM_EN is set, P2 SFR contains 00H, and R0 contains 30H, an access to the ARAM at address 30H will be performed.

If ARAM_EN is set, P2 SFR contains 01H, and R0 contains 30H, an access to the external memory address 0130H will be performed if P2 is connected to the high byte address bus of external RAM.

3.2 Dual Data Pointer

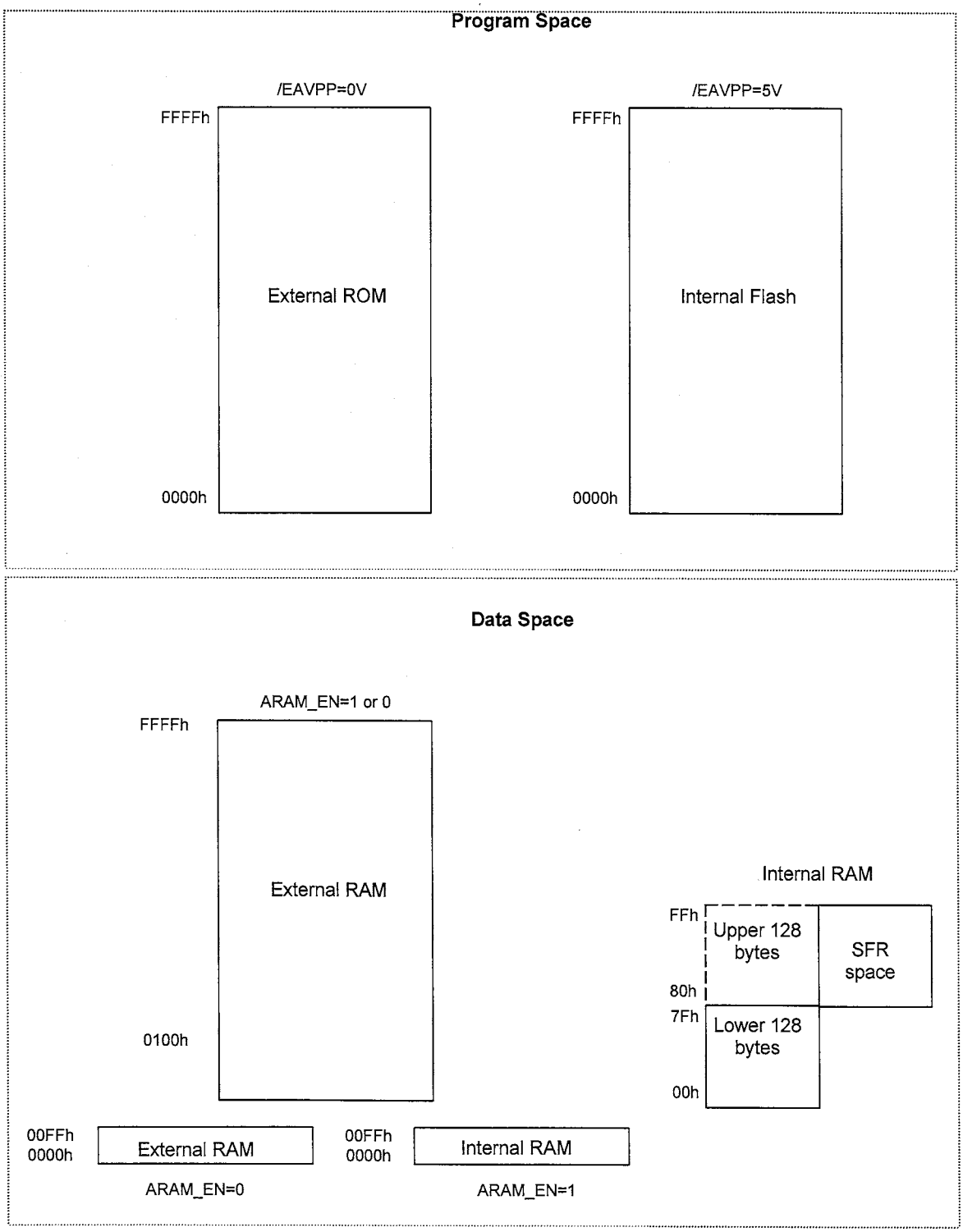
Data memory block moves can be accelerated using the Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the M6759, the standard 16-bit data pointer is called DPTR0 and is located at SFR address 82H and 83H. These are the standard locations. The new DPTR is located at SFR 84H and 85H and is called DPTR1. The new DPTR Select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86H. No other bits in register 86H have any effect and are set to 0. The user switches between data pointer by toggling the LSB of register 86H. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity.

3.3 Low EMI Mode

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purpose. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, setting bit 0 of SFR location 8EH can disable ALE operation. With the bit set, ALE is active only during a MOVX instruction. Otherwise the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the micro-controller is in external execution mode.

Memory Map


Program Space
/EAVPP=0V
FFFFh
External ROM
0000h
/EAVPP=5V
FFFFh
Internal Flash
0000h
Data Space
ARAM_EN=1 or 0
FFFFh
External RAM
0100h
Internal RAM
FFh
Upper 128 bytes
SFR space
80h
7Fh
Lower 128 bytes
00h
00FFh
0000h
External RAM
ARAM_EN=0
00FFh
0000h
Internal RAM
ARAM_EN=1

3.4 Idle Mode

In Idle mode, CPU put itself into sleep while all the on-chip peripherals remain active. The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. The content of RAM and special functions register remain unchanged, and the status of CPU (includes Stack Point, Program Counter, Program Status Word and Accumulator) is preserved in this mode.

There are two ways to terminate Idle mode:

- Activation of any enabled interrupt will cause IDLE (PCON.0) to be cleared by hardware terminating Idle mode. The interrupt will be serviced, and returned by instruction RETI. The next instruction to be executed is the one which follows the instruction that wrote a logic 1 to PCON.0. The flag bits GF0 (PCON.2) and GF3 (PCON.6) can be used to determine whether the interrupt was received during normal execution or during the Idle mode. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
- The second way of terminating the Idle mode is with an external hardware reset.

3.5 Power Down Mode

Setting PCON.1 (PD) can force CPU enter Power Down mode. In this mode, on-chip oscillator is stopped to save most of power. All functions are stopped due to the clock frozen, but the contents of RAM and special functions register are held.

To terminate Power Down mode, the only way is hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart stably.

3.6 Reset

The RST is the reset input, which is the input to a Schmitt Trigger. A reset is accomplished by holding the RST pin high for at least four oscillator periods while the oscillator is running. The CPU responds by generating an internal reset, with the timing shown in Reset Timing. The external reset signal is synchronous to the internal clock. The port pins will maintain high by internal pull-ups for 205 oscillator periods after RST pin goes low. While the RST pin is high, ALE and /PSEN are weakly pulled high. After RST is pulled low, it will take about 205 oscillator periods for ALE and PSEN to start clocking. For this reason, other devices can not be synchronized to the internal timings of the m6759. Driving the ALE and /PSEN pins to 0 while reset is active could cause the device to go into an indeterminate state.

The internal reset algorithm writes 0s to all the SFRs except the port latches, the Stack Pointer, and SBUF. The port latches are initialized to FFH, the Stack Pointer to 07H, and SBUF is indeterminate. The internal RAM is not affected by reset. On power up the RAM content is indeterminate.

3.7 Interrupt Processing

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt, as listed in Table 11. The CPU executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with a RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR can only be interrupted by a higher priority interrupt. That is, an ISR for a low-priority level interrupt can only be interrupted by high-priority level interrupt. An ISR for a high-priority level cannot be interrupted by any other interrupt.

M6759 always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI, or a write access to any of the IP or IE SFRs, M6759 completes one additional instruction before servicing the interrupt.

3.8 Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts. When EA=1, each interrupt is enabled/masked by its individual enable bit. When EA=0, all interrupts are masked.

3.9 Interrupt Priorities

There are two stages of interrupt priority assignment, interrupt level and natural priority. The interrupt level (high or low) takes precedence over natural priority. All interrupts can be assigned to be high or low priority. In addition to an assigned priority level, each interrupt also has a natural priority, as listed in Table 3-2. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if /INT0 and /INT1 are both programmed as high priority, /INT0 takes precedence.

Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

Mode	Program Memory	ALE	/PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Table 3-1. Status of the External pins During Idle and Power Down

Reset Timing

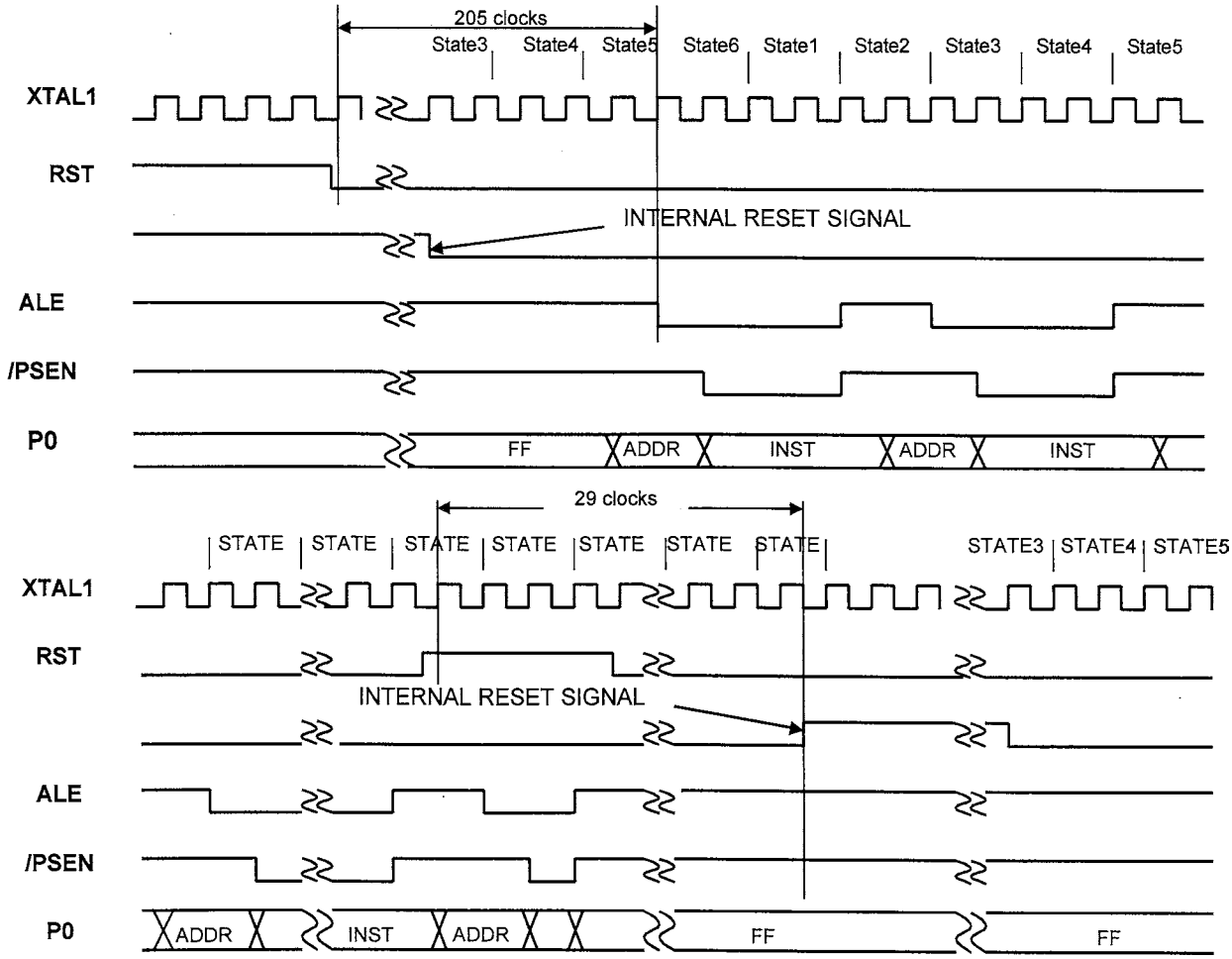


Table 3-2. Interrupt Natural Vectors and Priorities

Interrupt	Description	Natural Priority	Interrupt Vector
/INT0	External interrupt 0	0	03H
TF0	Timer 0 interrupt	1	0BH
/INT1	External interrupt 1	2	13H
TF1	Timer 1 interrupt	3	1BH
TI or RI	Serial Port transmit or receive interrupt	4	23H
TF2	Timer 2 interrupt	5	2BH

Table 3-3. Interrupt Flag, Enables and Priority Control

Interrupt	Description	Flag	Enable	Priority Control
/INT0	External interrupt 0	TCON.1	IE.0	IP.0
TF0	Timer 0 interrupt	TCON.5	IE.1	IP.1
/INT1	External interrupt 1	TCON.3	IE.2	IP.2
TF1	Timer 1 interrupt	TCON.7	IE.3	IP.3
TI or RI	Serial Port transmit or receive interrupt	SCON0.0	IE.5	IP.5
		SCON0.1		
TF2	Timer 2 interrupt	T2CON.7	IE.6	IP.6

4.0 SPECIAL FUNCTION REGISTERS

SFR Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
P0									80H
SP									81H
DPL0									82H
DPH0									83H
DPL1									84H
DPH1									85H
DPS	0	0	0	0	0	0	0	SEL	86H
PCON	SMOD	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	87H
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88H
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	89H
TL0									8AH
TL1									8BH
TH0									8CH
TH1									8DH
LEMI	0	0	0	0	0	0	0	LOWEMI	8EH
P1									90H
AUXR	ARAM_EN	GF6	GF5	*EB	*BRG1	*BRG0	*INT2I	*INT2E	97H
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	98H
SBUF									99H
P2									A0H
IE	EA	*EX2	ET2	ES0	ET1	EX1	ET0	EX0	A8H
P3									B0H
IP	1	*PX2	PT2	PS0	PT1	PX1	PT0	PX0	B8H
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	C8H
RCAP2L									CAH
RCAP2H									CBH
TL2									CCH
TH2									CDH
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0H
ACC									E0H
*P4									E8H
B									F0H
*P5									F8H

All register labeled with * can be only used in 68-pin package (not available now)

SFR Register Initial Value

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
P0	1	1	1	1	1	1	1	1	80H
SP	0	0	0	0	0	1	1	1	81H
DPL0	0	0	0	0	0	0	0	0	82H
DPH0	0	0	0	0	0	0	0	0	83H
DPL1	0	0	0	0	0	0	0	0	84H
DPH1	0	0	0	0	0	0	0	0	85H
DPS	0	0	0	0	0	0	0	0	86H
PCON	0	0	0	0	0	0	0	0	87H
TCON	0	0	0	0	0	0	0	0	88H
TMOD	0	0	0	0	0	0	0	0	89H
TL0	0	0	0	0	0	0	0	0	8AH
TL1	0	0	0	0	0	0	0	0	8BH
TH0	0	0	0	0	0	0	0	0	8CH
TH1	0	0	0	0	0	0	0	0	8DH
LEMI	0	0	0	0	0	0	0	0	8EH
P1	1	1	1	1	1	1	1	1	90H
AUXR	0	0	0	0	1	1	0	0	97H
SCON	0	0	0	0	0	0	0	0	98H
SBUF	0	0	0	0	0	0	0	0	99H
P2	1	1	1	1	1	1	1	1	A0H
IE	0	0	0	0	0	0	0	0	A8H
P3	1	1	1	1	1	1	1	1	B0H
IP	0	0	0	0	0	0	0	0	B8H
T2CON	0	0	0	0	0	0	0	0	C8H
RCAP2L	0	0	0	0	0	0	0	0	CAH
RCAP2H	0	0	0	0	0	0	0	0	CBH
TL2	0	0	0	0	0	0	0	0	CCH
TH2	0	0	0	0	0	0	0	0	CDH
PSW	0	0	0	0	0	0	0	0	D0H
ACC	0	0	0	0	0	0	0	0	E0H
P4	1	1	1	1	1	1	1	1	E8H
B	0	0	0	0	0	0	0	0	F0H
P5	1	1	1	1	1	1	1	1	F8H

Register Definition

4.1 CPU Control and Status Register

SFR 86H: DPS register, Data Pointer Select Register

Bit	Description
7-1	0
0	SEL. The DPTR Select bit. When SEL=0, DPTR0 is the active pointer. When SEL=1, DPTR1 is the active pointer.

SFR 87H: PCON Register, Power Control Register

Bit	Description
7	SMOD, Double Baud Rate bit. If Timer 1 is used to generate baud rate and SMOD=1, the baud rate is doubled when the Serial Port is used in modes 1, 2 or 3.
6-2	GF3–GF0, General Purpose Flag bit.
1	PD, Power Down bit.
0	IDLE, Idle Mode bit.

SFR 8EH: LEMI Register, Low EMI Control Register

Bit	Description
7-1	0
0	LOWEMI, The Low EMI Setting bit. If the M6759 operate in the internal access mode, ALE is active only during a MOVX instruction when LOWEMI=1.

SFR 97H: AUXR Register, Auxiliary Register

Bit	Description
7	ARAM_EN, Access Internal Auxiliary RAM Enable bit. When ARMA_EN=0, the access of external RAM will be performed by MOVX. When ARAM_EN=1, access internal auxiliary RAM rather than external RAM.
6-5	GF6-GF5. General Purpose Flag bit.
4-0	Reserved.

SFR D0H: PSW Register, Program Control Register

Bit	Description		
7	CY, Carry Flag. Set to 1 when the last arithmetic operation results in a carry into (during addition) or borrow from (during subtraction) the high order nibble. Otherwise, this bit is cleared to 0 by all arithmetic operations.		
6	AC, Auxiliary Carry Flag. Set to 1 when the last arithmetic operation results in a carry into (during addition) or borrow from (during subtraction) the high order nibble. Otherwise, this bit cleared to 0 by all arithmetic operations.		
5	F0, User Flag 0, user addressable. Generates purpose flag for software control.		
4-3	RS1-0, Register Bank Select		
	RS1	**RS0**	**Bank Selected**
	0	0	Register Bank 0, address 00h-07h
	0	1	Register Bank 1, address 08h-0Fh
	1	0	Register Bank 2, address 10h-17h
	1	1	Register Bank 3, address 17h-1Fh
2	OV, Overflow Flag. Set to 1 when the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise, this bit is cleared to 0 by all arithmetic operations.		
1	GF, User Flag 1, user addressable. Generator purpose flag for software control.		
0	F1, Parity Flag. Set to 1 when the modulo-2 sum of the 8 bits in the accumulator is 1 (odd parity), clear to 0 on even parity.		

Interrupt Registers

SFR A8H: IE Register

Bit	Description
7	EA, Global Interrupt Enable. Controls masking of all interrupts except power fail interrupt. EA=0 disable all interrupts (EA overrides individual interrupt enable bits). When EA=1, each interrupt is enabled or masked by its individual enable bit.
6	Reserved.
5	ET2, Enable External Timer 2. ET2=0 disables Timer 2 interrupt (TF2). ET2=1 enables interrupts generated by TF2 flag.
4	ES0, Enable Serial Port 0 Interrupt. ES0=0 disables Serial Port 0 interrupts (TI_0 and RI_0). ES0=1 enables interrupts generated by the TI_0 or RI_0 flag.
3	ET1, Enable External Timer 1. ET1=0 disables Timer 1 interrupt (TF1). ET1=1 enables interrupts generated by TF1 flag.
2	EX1, Enable External Interrupt 1. EX1=0 disables external interrupt 1 (/INT1). EX1=1 enables interrupts generated by /INT1.
1	ET0, Enable External Timer 0. ET0=0 disables Timer 0 interrupt (TF0). ET0=1 enables interrupts generated by TF0 flag.
0	EX0, Enable External Interrupt 0. EX0=0 disables external interrupt 0 (/INT0). EX0=1 enables interrupts generated by /INT0.

SFR B8H: IP Register

Bit	Description
7	Reserved, read as 1.
6	Reserved.
5	PT2, Timer 2 Interrupt Priority Control. PT2=0 sets Timer 2 interrupt (TF2) to low priority. PT2=1 sets Timer 2 interrupt to high priority.
4	PS0, Serial Port 0 Interrupt Priority Control. PS0=0 sets Serial Port 0 interrupts (TI_0 and RI_0) to low priority. PS0=1 sets Serial Port 0 to high priority.
3	PT1, Timer 1 Interrupt Priority Control. PT1=0 sets Timer 1 interrupt (TF1) to low priority. PT1=1 sets Timer 1 interrupt to high priority.
2	PX1, External Interrupt 1 Priority Control. PX1=0 sets external interrupt 1 (/INT1) to low priority. PX1=1 sets external interrupt 1 to high priority.
1	PT0, Timer 0 Interrupt Priority Control. PT0=0 sets Timer 0 interrupt (TF0) to low priority. PT0=1 sets Timer 0 interrupt to high priority.
0	PX0, External Interrupt 0 Priority Control. PX0=0 sets external interrupt 0 (/INT0) to low priority. PX0=1 sets external interrupt 0 to high priority.

4.2 Peripheral Device Registers

SFR 88H: TCON Register

Bit	Description
7	TF1, Timer 1 Overflow Flag. Set to 1 when Time 1 count overflows and clears when the processor vectors to the interrupt service routine.
6	TR1, Timer 1 Run Control. Set to 1 to enable counting on Timer 1.
5	TF0, Timer 0 Overflow Flag. Set to 1 when Time 0 count overflows and clears when the processor vectors to the interrupt service routine.
4	TR0, Timer 0 Run Control. Set to 1 to enable counting on Timer 0.
3	IE1, Interrupt 1 Edge Detect. If external interrupt 1 is configured to be edge sensitive (IT1=1), IE1 is set by hardware when a negative edge is detected on the /INT1 and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In this case, IE1 can also be cleared by software. If external interrupt 1 is configured to be level-sensitive (IT1=0), IE1 is set when /INT1 is 0 and cleared when /INT1 is 1. In level-sensitive mode, software can not write to IE1.
2	IT1, Interrupt 1 Type Selector, /INT1 is detected on falling edge when IT1=1; /INT1 is detected as a low level when IT1=0.
1	IE0, Interrupt 0 Edge Detect. If external interrupt 0 is configured to be edge sensitive (IT0=1), IE0 is set by hardware when a negative edge is detected on the /INT0 and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In this case, IE0 can also be cleared by software. If external interrupt 0 is configured to be level-sensitive (IT0=0), IE0 is set when /INT0 is 0 and cleared when /INT0 is 1. In level-sensitive mode, software can not write to IE0.
0	IT0, Interrupt 0 Type Selector, /INT0 is detected on falling edge when IT0=1; /INT0 is detected as a low level when IT0=0.

SFR 89H: TMOD Register

Bit	Description
7	GATE. Timer 1 Gate Control, when GATE=1, Timer 1 will clock when /INT1 and TR1 (TCON.6)= 1. When GATE=0, Timer 1 will clock only when TR1=1, regardless of the state of /INT1
6	C/T, Counter/Timer Selector, when C/T=0, Timer 1 is clocked by clk/12, depending on the state of T1M (CKCON.4). When C/T=1, Timer 1 is clocked by T1 pin.
5-4	M1-0, Timer 1 mode select bits **M1 M0 Mode** 0 0 Mode 0: 13 bit counter 0 1 Mode 1: 16 bit counter 1 0 Mode 2: 8 bit counter with auto-reload 1 1 Mode 3: off
3	GATE. Timer 0 Gate Control, when GATE=1, Timer 0 will clock when /INT0 and TR0 (TCON.4)= 1. When GATE=0, Timer 0 will clock only when TR0=1, regardless of the state of /INT0.
2	C/T, Counter/Timer Selector, when C/T=0, Timer 0 is clocked by clk/12, depending on the state of T0M (CKCON.3). When C/T=1, Timer 0 is clocked by T0 pin.
1-0	M1-0, Timer 0 mode select bits **M1 M0 Mode** 0 0 Mode 0: 13 bit counter 0 1 Mode 1: 16 bit counter 1 0 Mode 2: 8 bit counter with auto-reload 1 1 Mode 3: Two 8 bit counter

SFR C8H: T2CON Register

Bit	Description
7	TF2, Timer 2 Overflow Flag. Hardware will set TF2 when the Timer 2 overflow from FFFFH, TF2 must be cleared to 0 by software. TF2 will only be set to 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
6	EXF2, Timer 2 External Flag. Hardware will set EXF2 when a reload or capture is caused by a high-to-low transition on the T2EX pin, and EXEN2 is set. EXF2 must be cleared to 0 by software. Writing a 1 to EXF2 forces a Timer 2 interrupt if enable.
5	RCLK, Receive Clock Flag. Determine whether Timer 1 or Timer 2 is used for Serial Port 0 timing of receive data in serial mode 1 or 3. RCLK=1 selects Timer 2 overflow as the receive clock. RCLK=0 selects Timer 1 overflow as the receive clock.
4	TCLK, Transmit Clock Flag. Determine whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. RCLK=1 selects Timer 2 overflow as the transmit clock. RCLK=0 selects Timer 1 overflow as the transmit clock.
3	EXEN2, Timer 2 External Enable. EXEN2=1 enables capture or reload to occur as a result of high-to-low transition on T2EX, if Timer 2 is not generating baud rates for the serial port. EXEN2=0 causes Timer 2 to ignore all external events at T2EX.
2	TR2, Timer 2 Run Control Flag. TR2=1 starts Timer 2, TR2=0 stops Timer 2.
1	C/T2 Counter/Timer Selector. C/T2=0 selects a timer function for Timer 2. C/T2=1 selects a counter of falling transitions on the T2 pin. When used as a timer, Timer 2 run at 4 clocks per tick or 12 clocks per tick as programmed by CKCON.5, in all modes except baud rate generator mode. When used in baud rate generator mode, Timer 2 runs at 2 clocks per tick, independent of state of CKCON.5
0	CP/RL2, Capture/Reload Flag. When CP/RL2=1, Timer 2 captures occur on high-to-low transitions of T2EX, if EXEN2=1. When CP/RL2=0, auto-reloads occur when Timer2 overflows or when high-to-low transitions occur on T2EX, if EXEN2=1. If either RCLK or TCLK is set to 1, CP/RL2 will not function and Timer 2 will operate in auto-reload mode following each overflow.

SFR 98H: SCON Register

Bit	Description		
7-6	SM1, SM0, Serial Port 0 Mode Select bits		
	SM1	**SM0**	**Mode**
	0	0	0
	0	1	1
	1	0	2
	1	1	3

Bit	Description
5	SM2, Multiprocessor Communication Enable. In modes 2 and 3, this bit enables the multiprocessor communication feature. If SM2=1 in mode 2 or 3, the RI will not be activated if the received 9th bit is 0. If SM2=1 is in mode 1, then RI will only be activated if a valid stop is received. In mode 0, SM2 establishes the baud rate: when SM2=0, the baud rate is clk/12; when SM2=1, the baud rate is clk/4.
4	REN, Receive Enable. When REN=1, reception is enabled.
3	TB8, Defined the state of the 9th data bit transmitted in modes 2 and 3.
2	RB8, In modes 2 and 3, RB8 indicates the state of the 9th bit received. In mode 1, RB8 indicates the state of received stop bit. In mode 0, RB8 is not used.
1	TI, Transmit Interrupt Flag. Indicates that the transmit data word has been shifted out. In mode 0, TI is set at the end of the 8th data bit. In all other modes, TI is set when the stop bit is placed on the TXD pin, TI must be cleared by software.
0	RI, Receive Interrupt Flag. Indicates that serial data word has been received. In mode 0, RI is set at the end of the 8th data bit. In mode 1, RI is set after the last sample of the incoming stop bit, subject to the state of SM2. In modes 2 and 3, RI is set at the end of the last sample of RB8, RI must be cleared by the software.

5.0 Peripheral Device

5.1 Timer Operation

The M6759 has three 16-bit timer/counter registers, all three can be configured to operate either as timers or event counters.

When operating as timer function, the register increases by every machine cycle, each machine cycle consists of 12 oscillator periods. Thus, one can view the register as a counter with count rate 1/12 of oscillator frequency.

When operating as counter function, the register increases according to a 1-to-0 transition at corresponding external input pin, which can be T0, T1 or T2.

In this function, the external input pin is sampled at every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the counter increases by 1. Since it takes two machine cycles to determine a transition, the count rate is maximum 1/24 oscillator frequency. It is important that input signal should be held a given level at least one machine cycle to ensure the given level to be sampled. In addition to the timer/counter selection, Timer 0 and Timer 1 have four operating modes, Timer 2 has three operating modes. They are described below:

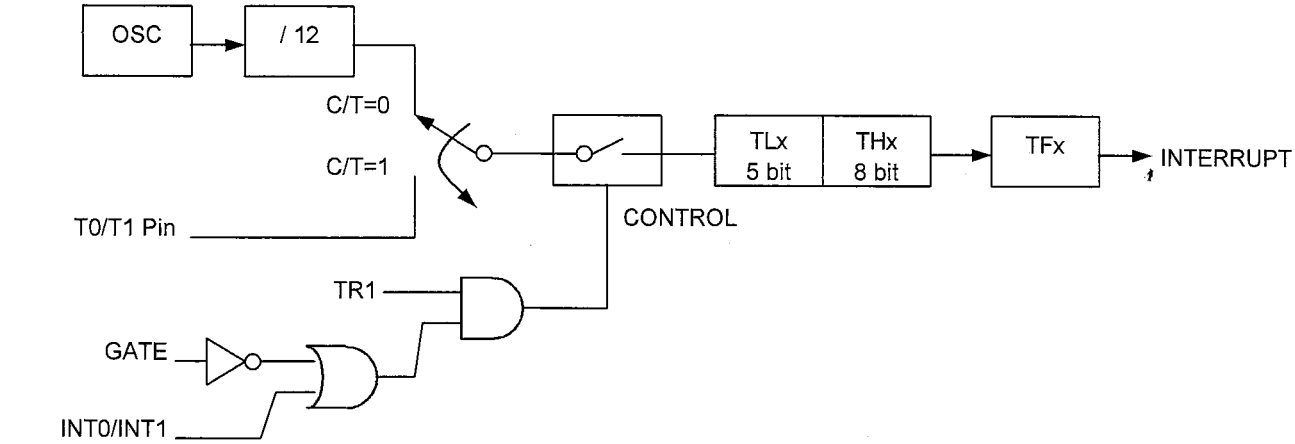
Timer0/Timer1 Mode Control

M1	M0	Operating Mode
0	0	8 bit Timer/Counter, "THx" with "TLx" as 5 bit prescaler
0	1	16 bit Timer/Counter, "THx" and "TLx" are cascadent
1	0	8 bit auto-reload timer/counter, each time "TLx" overflows, store value in "THx" into "TLx".
1	1	Timer 0 : TL0 and TH0 indicate two 8-bit counters controlled by Timer0 and Timer1 control bit Timer 1 : off

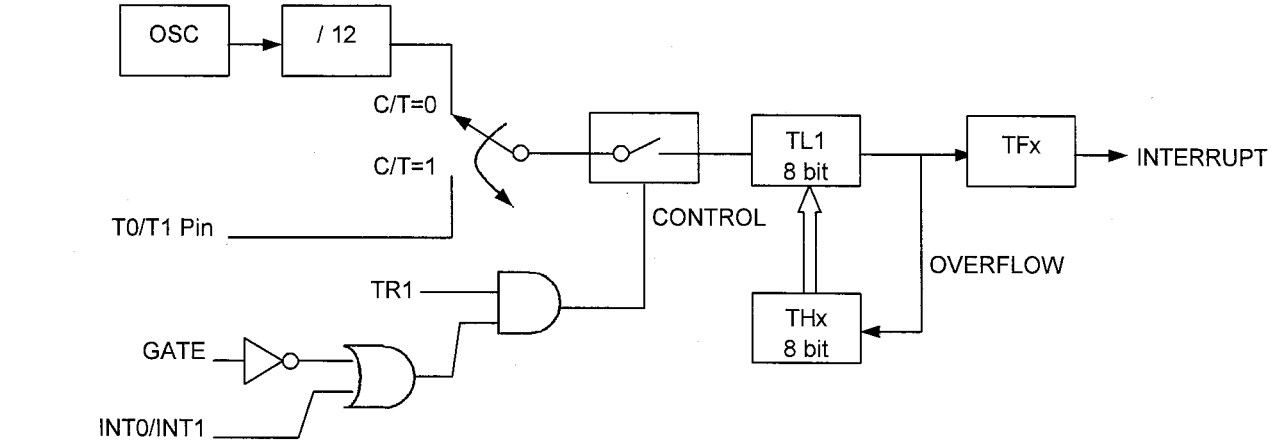
Timer2 Mode Control

RCLK + TCLK	CP/RL2	TR2	Operation Mode
0	0	1	16-bit auto-reload
0	1	1	16-bit capture
1	X	1	Baud rate generator
X	X	0	Non-active

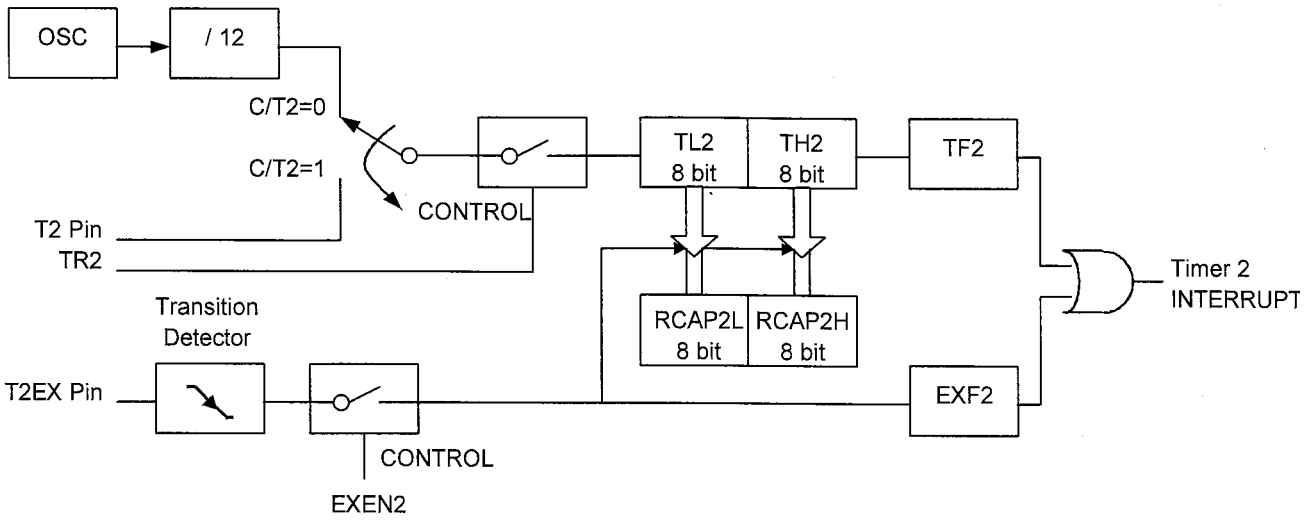
Timer/Counter Mode 0 : 13 bit Counter



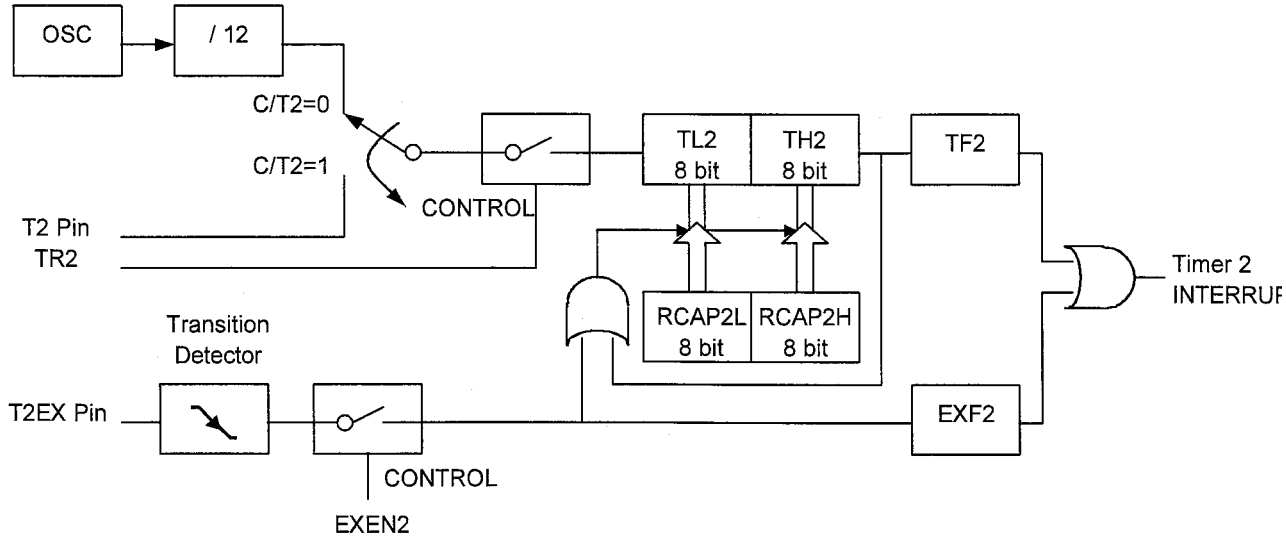
Timer/Counter Mode 2 : 8-bit Auto-Reload



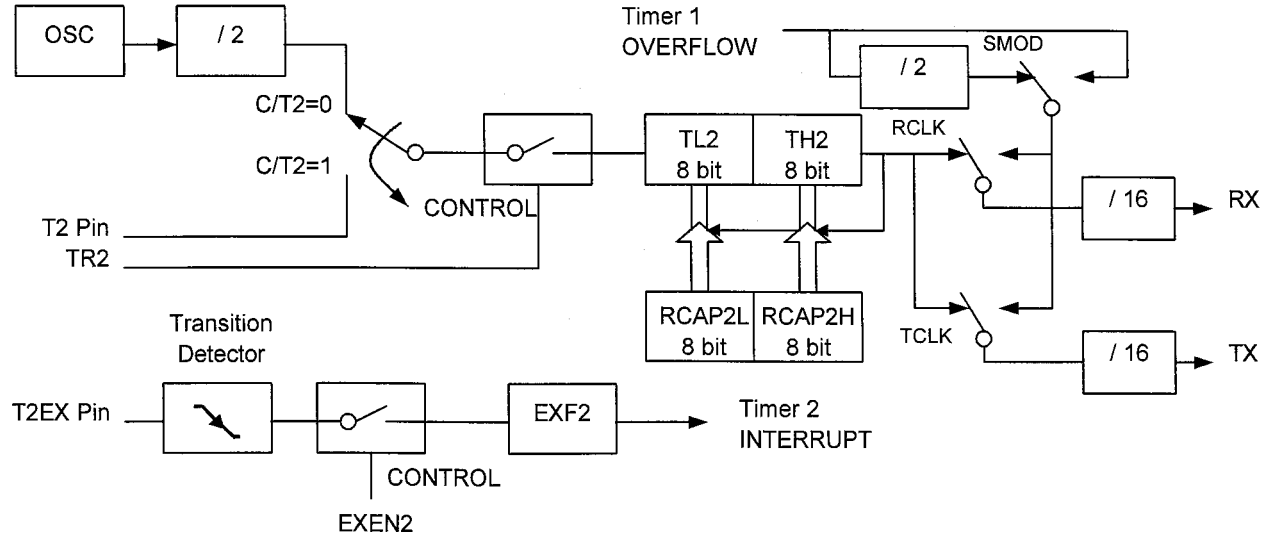
Timer 2 in Capture Mode



Timer 2 in Auto-reload Mode



Timer 2 In Baud Rate Generator Mode



Timer 2 is a 16-bit Timer/Counter. It can be selected as a timer or an event counter by register T2CON. It has three operating modes: "Capture", "Auto-reload" and "Baud rate generator".

In capture mode, there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 is 0, then Timer2 is a 16-bit timer/counter which sets bit TF2 (timer 2 overflow flag) upon overflowing, TF2 can generate an interrupt when Timer 2 interrupt is enabled. If EXEN2 is 1, above operation is still activated, with added feature that a 1-to-0 transition of external input pin T2EX can cause the content of TL2 and TH2 to be captured into RCAP2L and RCAP2H. In addition, the transition of T2EX set the bit EXF2 (which is in the T2CON register), and EXF2 can generate an interrupt.

In Auto-reload mode, there are two options that can be selected by bit EXEN2 in T2CON. If EXEN2 is 0, when Timer 2 overflows it sets TF2 and Timer 2 load the 16 bits values stored in RCAP2L and RCAP2H. If EXEN2 is 1, Timer2 still does the above, bit with an added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.

5.2 Serial Interface

The serial port is full duplex, which means it can transmit and receive data simultaneously. There is a receive buffer to commence reception second byte before previously received byte has been read from the receive register. (If the first byte has not been completely read by the time reception of the second byte, one of the bytes will still be lost). The serial port receive and transmit data are both accessed at SBUF. Writing to SBUF loads the transmit register. Read SBUF accesses a physically separate receive register.

Baud Rates

The Mode 0 Baud rate is fixed:

$$\textit{Rate Baud Mode} = \frac{\textit{Oscillator Frequency}}{12}$$

Baud rate in Mode 2 depends on the bit of SMOD in Special Function Register PCON. If SMOD is 0, baud rate is 1/64 of the oscillator frequency; if SMOD is 1, baud rate is 1/32 of the oscillator frequency.

$$\textit{Mode2 Baud Rate} = \frac{2^{SMOD} \text{ X } (\textit{Oscillator Frequency})}{64}$$

The Baud rate in Mode 1 and Mode 3 can be determined by overflow rate of Timer 1, Timer 2 or both (one for transmit and other for receive).

When Timer 1 is used to generate Baud rate, it is determined by following equation:

$$\text{Baud Rate} = \frac{2SMOD}{32} \text{ X (Timer1Overflow Rate)}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either timer or counter in any of its three running modes.

In the Auto-reload mode (high nibble of TMOD = 0010B), the baud rate is given by:

$$\text{Mode (1,3) Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{\textit{Oscillator Frequency}}{12x(256-TH1)}$$

When Timer 2 is used to generate Baud rate, it is set by TCLK and/or RCLK in T2CON, and the baud rate for transmit and receive can be different.

The baud rate generator mode is similar to the auto reload mode. A rollover in TH2 cause Timer 2 to be reload with 16 bit value which stored in RCAP2H and RCAP2L.

$$\text{Mode (1,3) Baud Rate} = \frac{\textit{Timer2 Overflow Rate}}{16}$$

The Timer can be configured for either "timer" or "counter" operation. Normally, as a timer it increments every machine cycle (12 oscillator cycles), as a baud rate generator it increments every state time (2 oscillator cycles). In that case baud rate is give by the following formula:

$$\text{Mode (1,3) Baud Rate} = \frac{\textit{Oscillator Frequency}}{32 \times [65536 - (RCAP2H, RCAP21L)]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and PCAP2L taken as a 16 bit unsigned integer which is preset by software.

Timer 2 in baud rate generator mode is valid only if RCLK or TCLK in T2CON is 1. The rollover in TH2 does not set TF2, and will not generate interrupt Also note that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L). In this case, T2EX can be used as an extra external interrupt if desire.

Timer 1 Reload Values Common Serial Port Mode 1 Baud Rates

Desired Baud Rate	SMOD	C/T	Timer 1 Mode	TH1 Value for 33 MHz clock	TH1 Value for 25 MHz clock	TH1 Value for 11.0592 MHz clock
57.6 Kb/s	1	0	2	FDH	FEH	FFH
19.2 Kb/s	1	0	2	F7H	F9H	FDH
9.6 Kb/s	1	0	2	EEH	F2H	FAH
4.8 Kb/s	1	0	2	DCH	E5H	F4H
2.4 Kb/s	1	0	2	B8H	CAH	E8H
1.2 Kb/s	1	0	2	71H	93H	D0H

Timer 2 Reload Values Common Serial Port Mode 1 Baud Rates

Desired Baud Rate	C/T2	33 MHz clock		25 MHz clock		11.0592 MHz clock	
		RCAP2H	RCAP2L	RCAP2H	RCAP2L	RCAP2H	RCAP2L
57.6 Kb/s	0	FFH	EEH	FFH	F2H	FFH	FAH
19.2 Kb/s	0	FFH	CAH	FFH	D7H	FFH	EEH
9.6 Kb/s	0	FFH	95H	FFH	AFH	FFH	DCH
4.8 Kb/s	0	FFH	29H	FFH	5DH	FFH	B8H
2.4 Kb/s	0	FEH	52H	FEH	BBH	FFH	70H
1.2 Kb/s	0	FCH	A5H	FDH	75H	FEH	E0H

6.0 Electrical Specifications

6.1 D.C. Characteristics

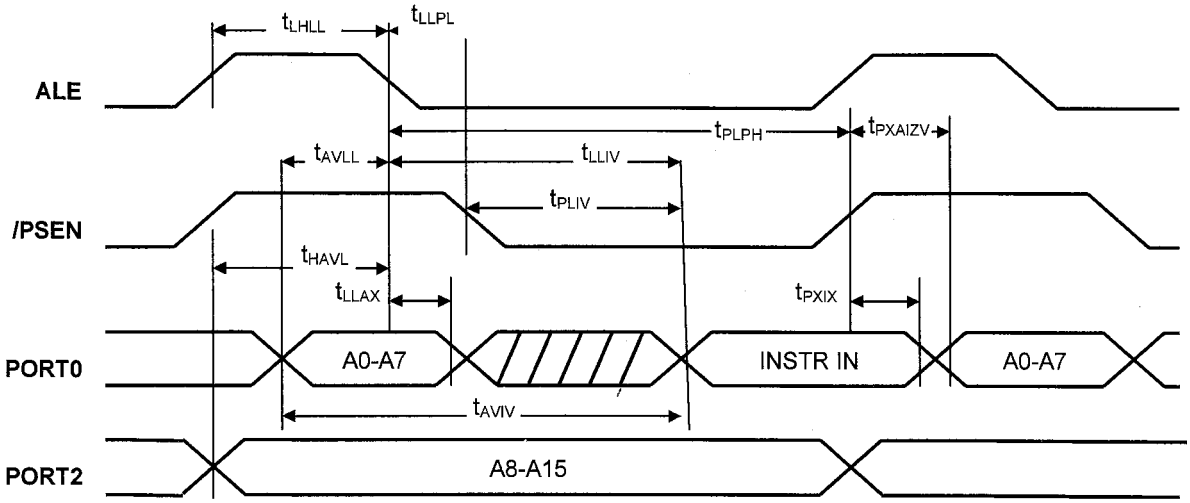
SYMBOL	PARAMETERS	MIN	MAX	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.4	$^{V}CC^{+0.5}$	V	
V_{OL}	Output Low Voltage	-	0.5	V	I_{OL}=4.0 mA
V_{OH}	Output High Voltage	4.0	-	V	I_{OH}= -4.0mA
I_{CC}	Power Supply Current Active mode	-	30	mA	VDD=5V Frequency=10MHz

6.2 AC Characteristics

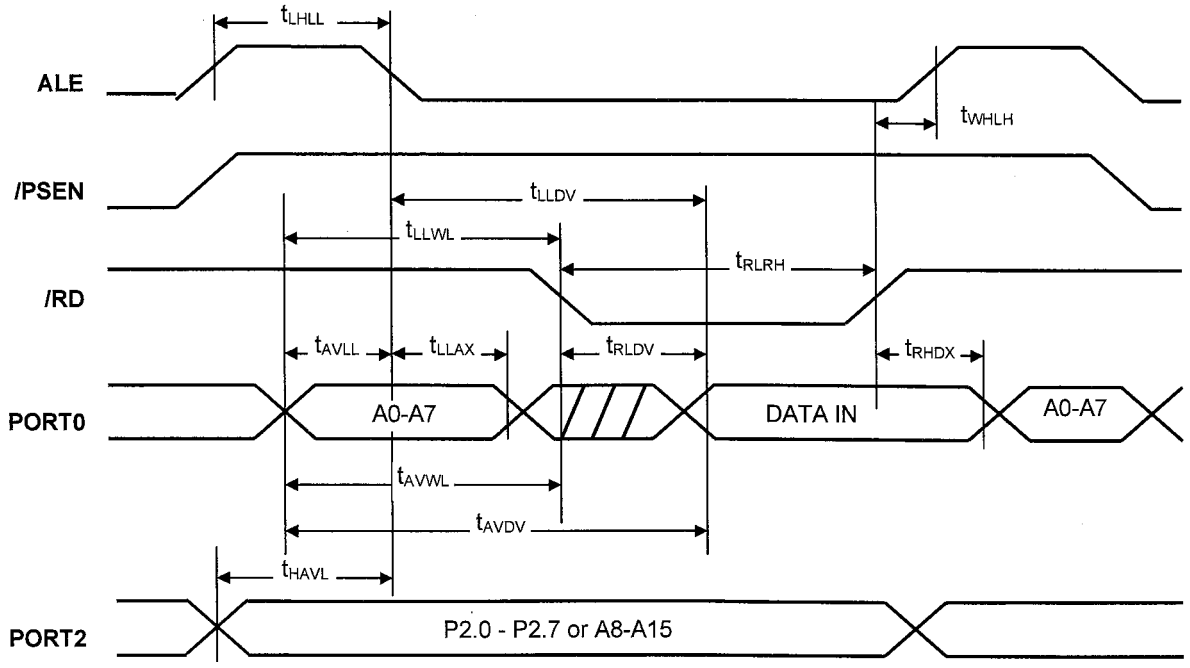
SYMBOL	PARAMETERS	MIN	MAX	Unit
t_{CLCL}	Oscillator Clock Cycle Period	25	-	ns
1 / t_{CLCL}	Oscillator Frequency	0	40	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL} – 40$	-	ns
t_{HAVL}	High bytes Address Valid to ALE Low	$2t_{CLCL} – 55$	-	ns
t_{AVLL}	Address Valid to ALE Low	$t_{CLCL} – 55$	-	ns
t_{LLAX}	Address Hold After ALE Low	$t_{CLCL} – 35$	-	ns
t_{LLIV}	Address Low to Valid Instruction In	-	$4t_{CLCL} – 100$	ns
t_{LLPL}	ALE Low to /PSEN Low	$t_{CLCL} – 40$	-	ns
t_{PLPH}	PSEN Pulse Width	$3t_{CLCL} – 45$	-	ns
t_{PLIV}	/PSEN Low to Valid Instruction In	-	$3t_{CLCL} – 105$	ns
t_{PXIX}	Input Instruction Hold After /PSEN	0	-	ns
t_{PXIZ}	/PSEN to Address Valid	-	t_{CLCL} - 25	ns
t_{AVIV}	Address to Valid Instruction In	-	$5t_{CLCL}$ - 105	ns
t_{RLRH}	/RD Pulse Width	$6t_{CLCL} – 100$	-	ns

SYMBOL	PARAMETERS	MIN	MAX	Unit
t_{WLWH}	/WR Pulse Width	$6t_{CLCL} - 100$	-	ns
t_{RLDV}	/RD Low to Valid Data In	-	$5t_{CLCL} - 165$	ns
t_{RHDX}	Data Hold After /RD	0	-	ns
t_{LLDV}	ALE Low to Data Valid In	-	$8t_{CLCL} - 150$	ns
t_{AVDV}	Address to Valid Data In	-	$9t_{CLCL} - 165$	ns
t_{LLWL}	ALE Low to /RD or /WR Low	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
t_{AVWL}	Address to /RD or /WR Low	$4t_{CLCL} - 130$	-	ns
t_{QVWX}	Data Valid to /WR Transition	$t_{CLCL} - 60$	-	ns
t_{QVWH}	Data Valid to /WR High	$7t_{CLCL} - 150$	-	ns
t_{WHQX}	Data Hold After /WR	$t_{CLCL} - 50$	-	ns
t_{WHLH}	/RD or /WR high to ALE High	-	$t_{CLCL} + 40$	ns

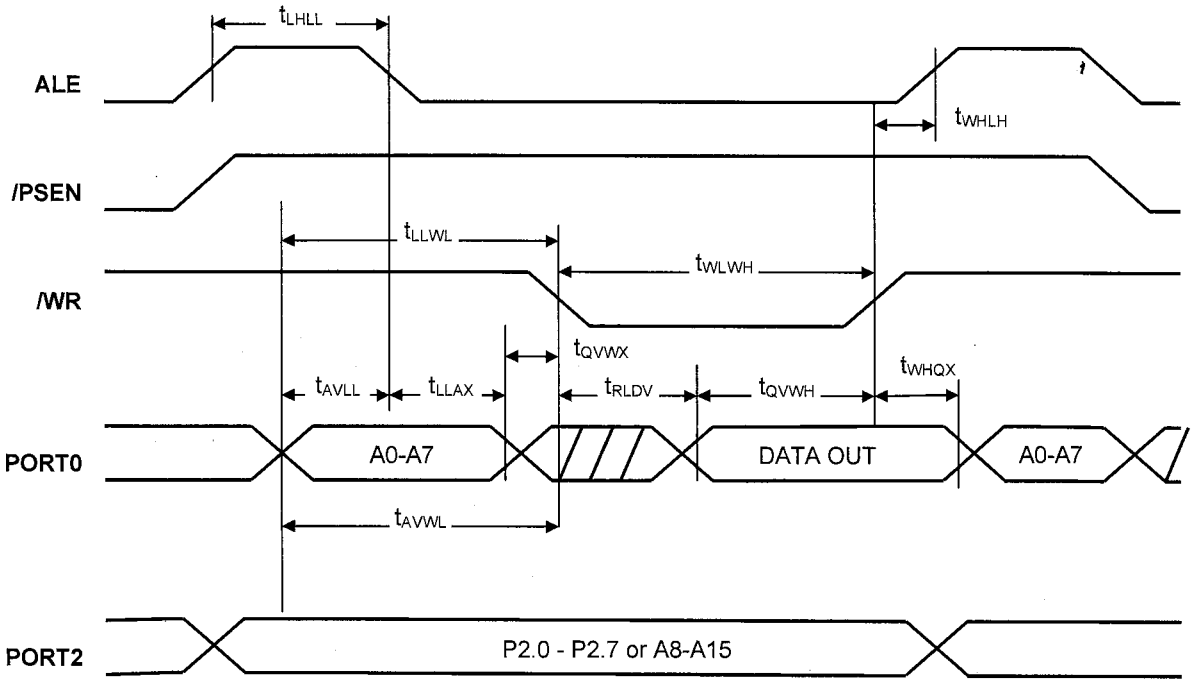
External Program Memory Read Cycle



External Data Memory Read Cycle



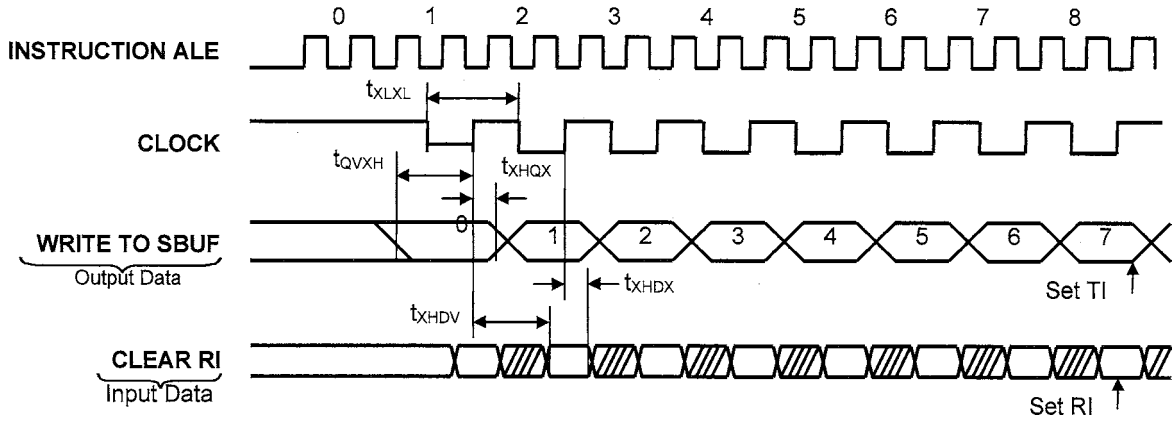
External Data Memory Write Cycle



Serial Port Timing : Shift Register Mode Test Conditions

SYMBOL	PARAMETER	MIN	MAX	Unit
t_{XLXL}	Serial Port Clock Cycle Time	12 t_{CLCL}	-	ns
t_{QVXH}	Output Data Setup to Clock Rising Edge	$9t_{CLCL} - 100$	-	ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	$3t_{CLCL} - 100$	-	ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0	-	ns
t_{XHDV}	Clock Rising Edge to Input Data Valid	-	$10t_{CLCL} - 133$	ns

Shift Register Mode Timing Diagram



7.0 Flash Programming Guide

Features

- 64 Kbytes electrically erasable internal program memory
- Encrypted verifiable
- 3-level program memory lock
- 100 program/erase cycles
- Fully synchronous operation
- High performance CMOS – 100ns read access time
- 12v external programming voltage

7.1 Description

The flash module is completely synchronous. All the operations are synchronized to the rising edge of the clock (XTAL1 pin). On the rising edge of the XTAL1, the pins' status is sampled and latched. For writing internal registers operations, the latched information is decoded during the XTAL1 high period, and execution is carried out on the falling XTAL1 edge. The flash module executes commands using an eight bit Instruction Register (IR), that defines the operation to be executed. Using the IR enables reading, programming and erasing main array and OTPR. The IR command is defined as the following table.

Table 7-1. IR Command Definition

Command	Code
Read Array	00h
Read OTPR (Key bytes or lock bits)	08h
Erase Array	80h
Erase OTPR (Key bytes or lock bits)	88h
Program Array	40h
Program OTPR (Key bytes or lock bits)	48h

There are two modules in the flash – main array and OTPR.

Main Array

The module' s main array contains 64K bytes of memory that serve as the code storage space for program code. The array occupies address space from 0000H to FFFFH.

OTP Rows

These non-volatile cells contain 2K bytes of memory that serve as a special storage space for protection data (i.e. key bytes and lock bits).

Note : Pin assignments shown below are listed based on 44-pin PLCC package. As for QFP package, the pin number assignment should be shifted accordingly, as comparatively shown in Section 2.1 Pinout Diagram.

Pin No. (PLCC)	Pin Name	Signal Name	Type	Description
44	VDD		IN	Power supply for internal operation, 5V input
22	GND		IN	Ground
35	/EA	Vpp	IN	Always hold 12V during erase, programming and read flash module
10, 33, 18	RST, ALE, P3.6	High	IN	Always hold high during erase, programming and read flash module
13, 14, 32	P3.1, P3.2, /PSEN	Low	IN	Always hold low during erase, programming and read flash module
31, 30, 29, 28, 27, 26, 25, 24	P2.7 to P2.0	A15 to A8	IN	Input high-order address bits
9, 8, 7, 6, 5, 4, 3, 2	P1.7 to P1.0	A7 to A0	IN	Input low-order address bits
36, 37, 38, 39, 40, 41, 42, 43	P0.7 to P0.0	D7 to D0	IN/OUT	Command/Data bus
11	P3.0	/RESET	IN	Flash reset
15	P3.3	IR_EN	IN	Instruction register access enable
16	P3.4	RDY	OUT	Ready signal
17	P3.5	/OE	IN	Output enable
19	P3.7	RD/WR_b	IN	Read/write selection

Program Lock Bits

The M6759 has 3 programmable lock bits that when programmed according to Table 7-2 will provide different levels of protection for the on-chip code and data. The lock bits are in the bit 4, bit 5 and bit 6 of OTPR address 0004. Refer to Figure 7-1 - OTPR arrangement.

Table 7-2. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	1	1	1	No Program Lock features enabled. (Code verify will be encrypted by the Encryption Array if programmed.)
2	0	1	1	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the flash is disabled.
3	0	0	1	Same as 2, also verify is disabled.
4	0	0	0	Same as 3, also external execution is disabled.

Encryption Array (key bytes)

There are 4 bytes of encryption array that are initially unprogrammed (all 1' s). Every time that a byte is addressed during verify, 2 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR' ed (XNOR) with the code byte, creating an encryption verify byte. The key bytes are in the address 0000, 0001, 0002 and 0003 of OTPR space.

The encryption function is available only when LB1 is programmed.

Status Bits

There are two status bits to constrain protection function in M6759. After whole chip is erased (include array and OTPR), ST0 must be programmed to 0. After key bytes and lock bits are programmed, ST1 must be programmed to 0. The status bits are in the bit1 and bit 0 of OTPR address 0004.

Status bits	Program Condition
ST0	The bit needs to be programmed after erased.
ST1	The bit needs to be programmed after protection function bytes (lock bits, key bytes) is programmed

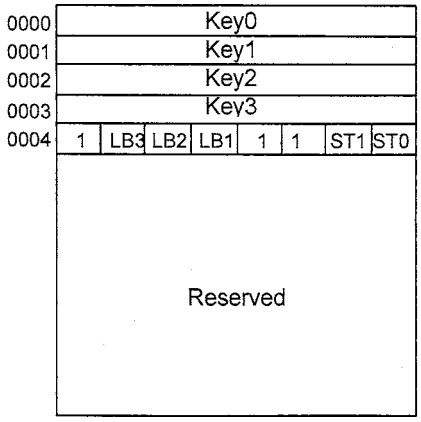


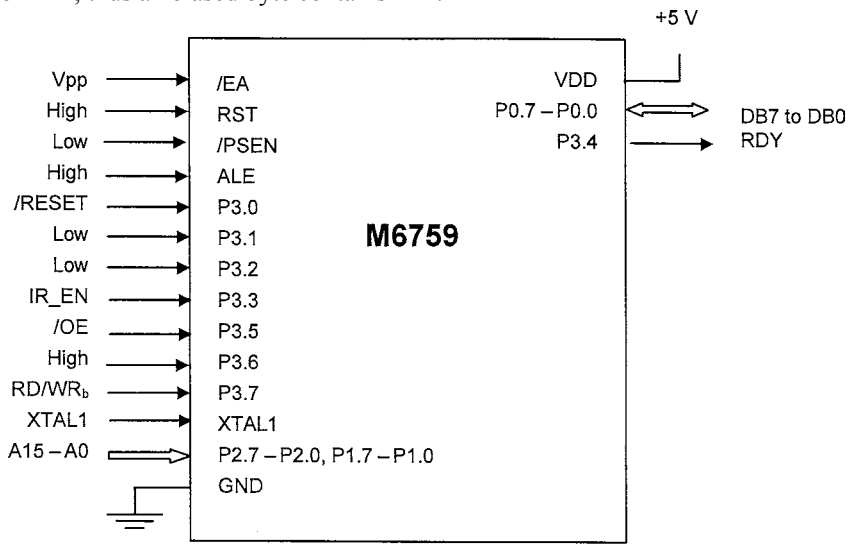
Figure 7-1. OTPR Arrangement Map

Programming

This mode enables the user to program the main memory and verify its contents. It also allows programming the OTPR. The cells to be programmed are defined by the IR command. In order to program, the required address is applied to the address bus, the required data byte is applied to the data bus and an IR program/verify instruction is executed. /OE signal must be set to high in order to avoid bus contention. This mode is operated through the Instruction Register, and requires the IR to be loaded prior to execution. Several programming pulses may be required to program a cell. Note that in order to succeed in programming, a byte must be fully erased prior to programming it. Erased byte holds the value of FFh. A written bit holds a value of zero. When programming is started. The RDY signal becomes low and remains low until the programming is over. During the period in which RDY signal is low, the module logic inputs are not sampled. The clock signal must be kept during RDY pin low period to ensure RDY is synchronized with the clock signal. Verify operation should be done following each byte programming. It is a read operation with built in margins performed using the IR (RD/WRb is high). If the verify fails, an additional programming cycle must be applied to the same address. Programming failure to a specific address is defined as 30 consecutive attempts to program the same address without a successful verify.

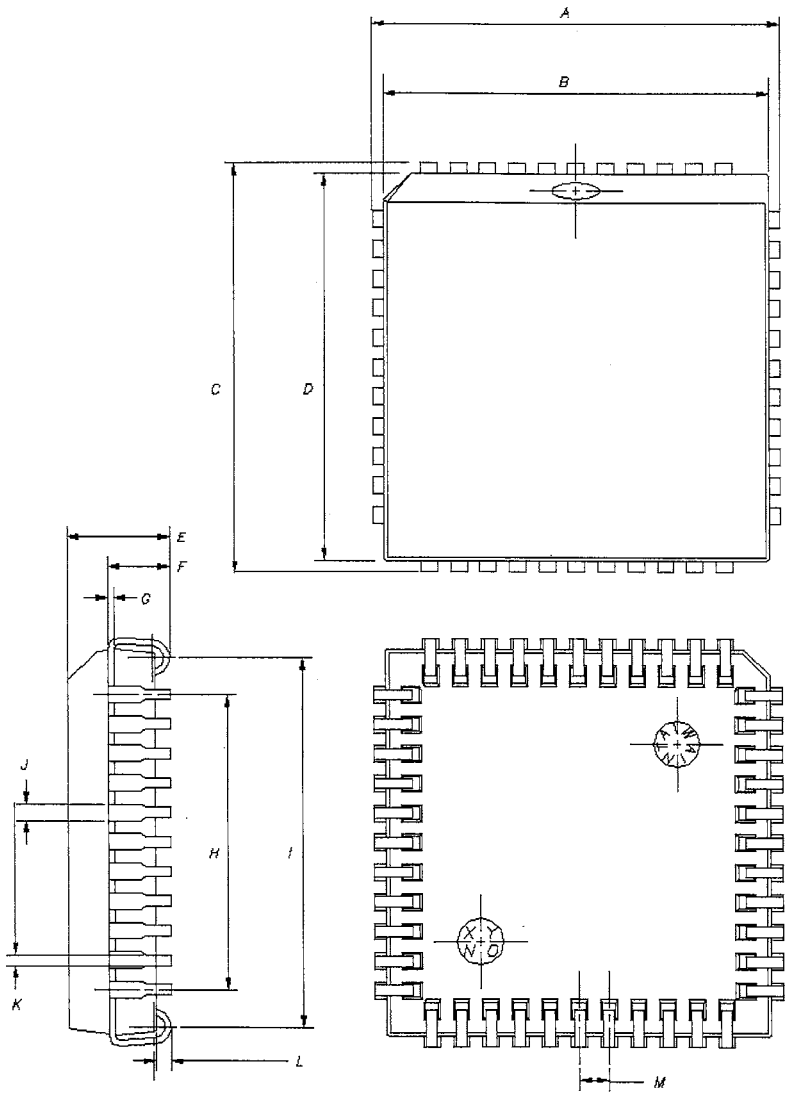
Erasing

This mode enables the user to erase the array and the OTPR. The cells to be erased are defined by the IR command. The command is executed upon the rising edge of the XTAL1, following writing the erase command into the IR. During erase, /OE signal must be high to avoid bus contention. The RDY signal becomes low and remains low until the erase operation is over. During the period in which RDY signal is low, the module logic inputs are not sampled. The clock signal must be kept during RDY pin low period to ensure RDY is synchronized with the clock signal. Verify procedure is a read operation with built in margins, required to confirm that all the word were successfully erased. To perform verify the user must revert the RD/WRb state to high, and apply an address to the address bus. Verify is carried out on the following rising edge of the XTAL1 signal. All addresses have to be applied sequentially in order to verify the entire array. During verify, /OE must be low to enable reading the erased cells. An erased cell has a value of ‘ 1’ ; thus an erased byte contains FFh.



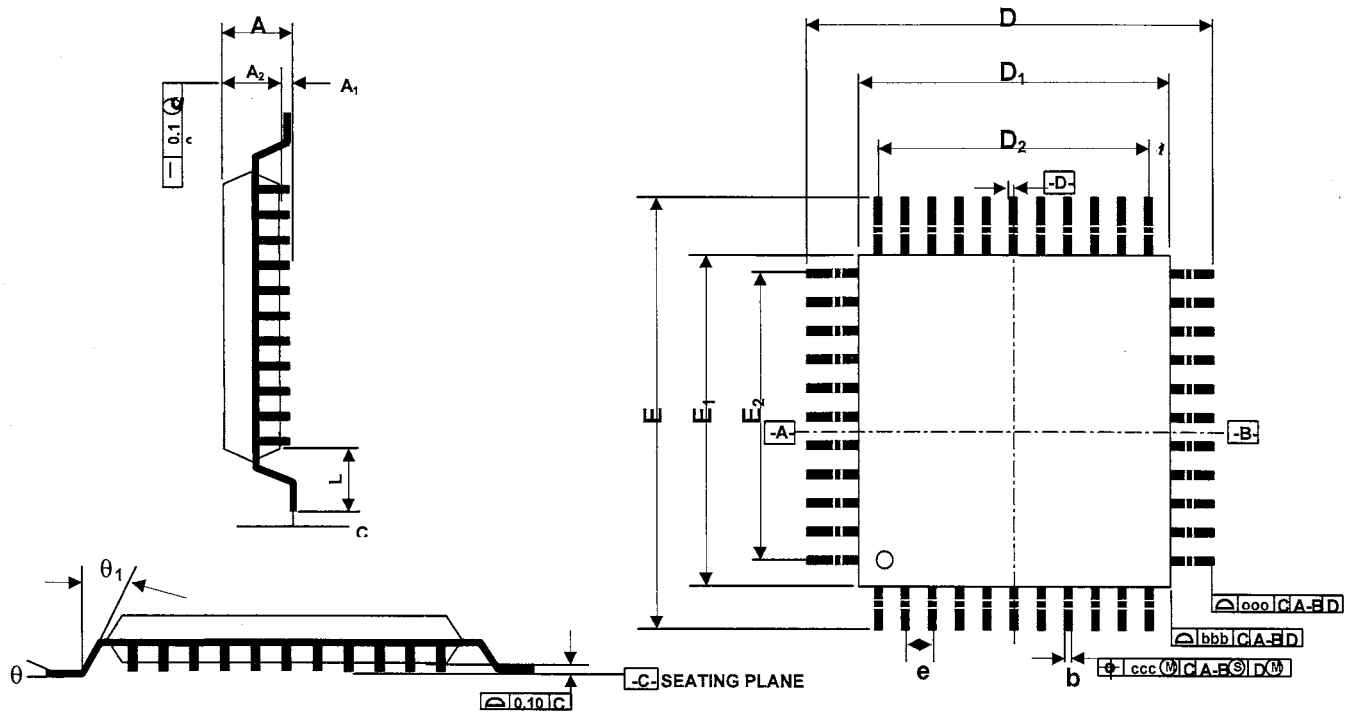
8.0 Packaging Information

44-pin PLCC Package



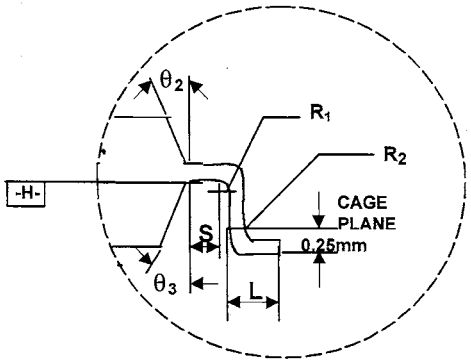
SYMBOL	Dimension in Inches			SYMBOL	Dimension in Inches		
	Min	Typ	Max		Min	Typ	Max
A	0.685	0.690	0.695	H	-	0.5	-
B	0.650	0.653	0.656	I	0.595	0.610	0.625
C	0.685	0.690	0.695	J	0.026	-	0.032
D	0.650	0.653	0.656	K	0.013	-	0.021
E	0.168	0.174	0.180	L	0.02	-	0.04
F	0.102	0.105	0.108	M	0.045	0.05	0.055
G	-	0.010	-				

44-pin QFP Package



CONTROL DIMENSIONS ARE IN MILLIMETERS

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.55	-	-	0.100
A_1	0.15	0.25	0.35	0.006	0.010	0.014
A_2	1.90	2.05	2.20	0.075	0.081	0.087
D	13.20 BASIC			0.520 BASIC		
D_1	10.00 BASIC			0.394 BASIC		
E	13.20 BASIC			0.520 BASIC		
E_1	10.00 BASIC			0.394 BASIC		
R_2	0.13	-	0.30	0.005	-	0.012
R_1	0.13	-	-	0.005	-	-
θ	0°	-	7°	0°	-	7°
θ_1	0°	-	-	0°	-	-
θ_2	10° REF			10° REF		
θ_3	7° REF			7° REF		
c	0.10	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.80			0.063		
c	0.10	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.80			0.063		
S	0.20	-	-	0.008	-	-

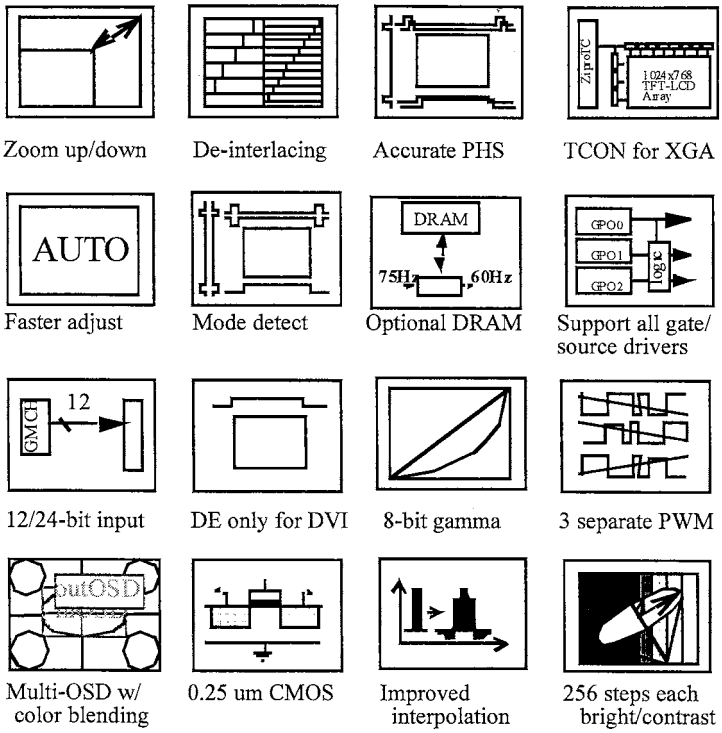


Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	8.0			0.315		
E2	8.0			0.315		
ooo	0.25			0.010		
bbb	0.20			0.008		
ccc	-	0.20	-	-	0.008	-

NOTES : 1, DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE (-H-). 2, DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL. IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

T0947 SCALER IC FPR XGA/SXGA LCD MONITORS

SPECIFICATION



1.0 INTRODUCTION

This datasheet contents the specification of ZiproSX (or t0947) and ZiproTC2 (t0949) chip for LCD monitor and LCD TV applications.

ZiproSX chip is pin-to-pin compatible with t0944 Zipro (Zoom engine for Interlaced to PROgressive scan) chip with a slightly modification in register programming. ZiproTC2 is pin-to-pin compatible with t0946 ZiproTC chip.

ZiproSX chip is targeted for XGA and SXGA interface and control of TFT-LCD while ZiproTC2 (Zipro with Timing Control V.2) is designed for smart-panel/smart-integration systems of SVGA/XGA display.

ZiproSX and ZiproTC2 chips convert PC/Mac/SUN and TV/HDTV video signals for flat panel display. It performs image scaling on true color RGB or YUV data stream and feeds the scaled pixels to LCD panel. It includes a SDRAM controller for frame rate conversion and interlace to progressive video processing. Besides, the chip contains an OSD (On Screen Display) logic with an overlay port for external OSD signals interface. An auto adjustment function provides automatic frequency, phase, H&V position, and white balance tuning at any screen condition. With no user intervention, the auto adjustment feature offers the jitter-free and best display quality while users display modes changed. Both ZiproSX and ZiproTC2 chips also contain display mode auto detection circuitry which provides accurate H and V timing detection for VESA, Sync-On-Green, and TV/HDTV signals.

To meet the market requirements of low cost, low power, and high level of integration, ZiproTC2 includes the improved timing control circuit for handling gate and source driver ICs for SVGA/XGA TFT-LCD panel directly. This solution, so called smart-panel/smart-integration system, can save the cost of connectors and cable between interface-board and LCD panel module. It also helps to reduce the EMI issue and hence provide the best performance/cost solution for flat panel displays.

ZiproSX (t0947) comes with 128-pin LQFP, 160-pin LQFP and 160-pin PQFP while ZiproTC2 (t0949) is packed in a 160-pin LQFP.

2.0 New Features

- Embedded controller 4M*16 as well as 1M*16 SDRAM
- Improved OSD (as t8570) for LCD/PDP user interface.
- Double-buffering mechanism for frame-rate conversion with no frame tear.
- The 2nd generation TCON for the 1st-time-right smart-panel control.
- Peaking and noise-reduction circuits for video enhancement.
- Improved dithering function for 8-bit to 6-bit conversion on all LCD panels.
- Improved PWM (Pulse-Width-Modulation) for more versatile analog control.
- Hardware display mode detection for HDTV signal.
- Color space conversion for TV and HDTV (ITU BT 601 and SMPTE 240M).
- Auto increment of address counter for JPEG/bitmap port.
- Improved Gamma table programming with programmable initial address.

2.1 General Features

- Embedded SDRAM controller for interlaced to progressive video and frame-rate conversion.
- On chip programmable OSD for user interface.
- Embedded hardware for display mode detection.
- Auto adjustment for frequency, phase, H/V position, and white balance.
- On chip brightness, contrast, and gamma correction.
- Max pixel rate up to 135 MHz.
- Embedded timing control circuit for source/gate drivers of SVGA/XGA TFT-LCD panel.
- Three PWMs (Pulse Width Modulators) for general purpose control.
- Integrated PLL for panel clock generation.
- 0.25 um CMOS technology with 5V tolerance input pads.

2.2 Input for ZiproSX and ZiproTC2

- 12-bit GMCH interface with external level-shifters.
- 24-bit RGB input up to 135MHz.
- 8-bit YUV 4:2:2 (CCIR 656), 16-bit YUV 4:2:2, and 24-bit YUV 4:4:4 video input. Glueless connection to video sources from ADC, MPEGII decoder or video decoder.
- Build-in YUV to RGB color space converter.
- Support for Sync-On-Green (SOG) and composite sync mode.
- 5V tolerance input pads support 5V/3.3V interface.

2.3 Scaler, and de-interlacer

- Anti-moiré high-quality scaling algorithm.
- Scaling up and down with filters for different sharpness.

2.4 Operating modes

- Scaling with no external SDRAM.
- De-interlacing and frame-rate conversion with external SDRAM.

2.5 Gamma correction and OSD

- 8-bit Gamma table.
- Downloadable 64-font RAM for user programmable and graphics fonts.
- Predefined 192-font ROM.
- Overlay port interface and color look-up table with 4 color indices (for anti-aliasing font and palette) from external OSD chip.
- Support the pixel-based pattern filling with a graphic port.

2.6 Output

- Single pixel/clock (24 bit) or double pixels/clock (48 bit) digital RGB output.
- Maximum resolution of color display is 1280*1024 (SXGA).
- Free-run synchronization mode if sync signal disappeared.
- Compliant with proposed VESA FPDI-2 standard via direct connect to LVDS transceivers.

2.7 System software and support

- Windows based OSD font and GUI design software.
- HDTV display and LCD multi-sync monitor system software.
- Scaler programming timing table for all VESA/MAC/Workstation and TV/HDTV.

2.8 Applications

- High resolution TFT-LCD or smart-panel LCD monitors.
- Set-top box and DVD player to LCD/PDP display devices.
- NTSC/PAL projection systems for office presentation and home theater.
- LCOS or OLED displays for HMD applications.
- Image scaling for video format conversions.

FIGURE 1. Typical application of ZiproSX/ZiproTC2 chip

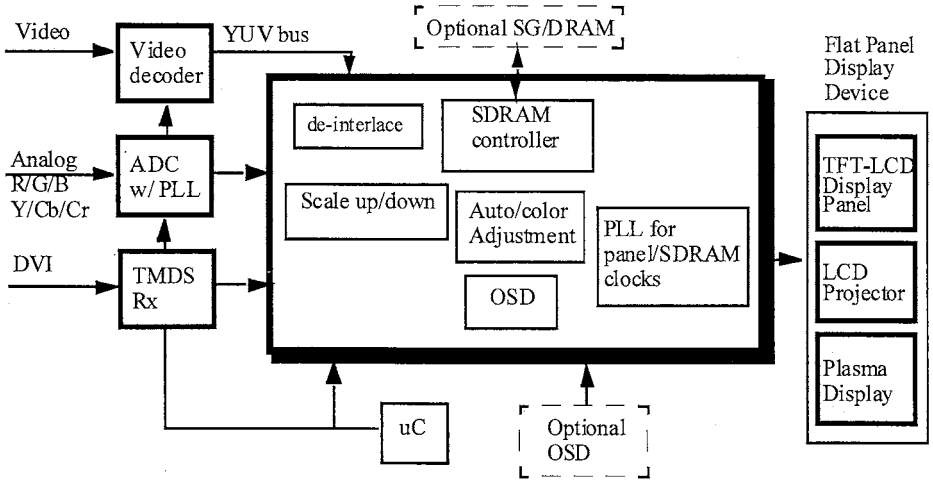
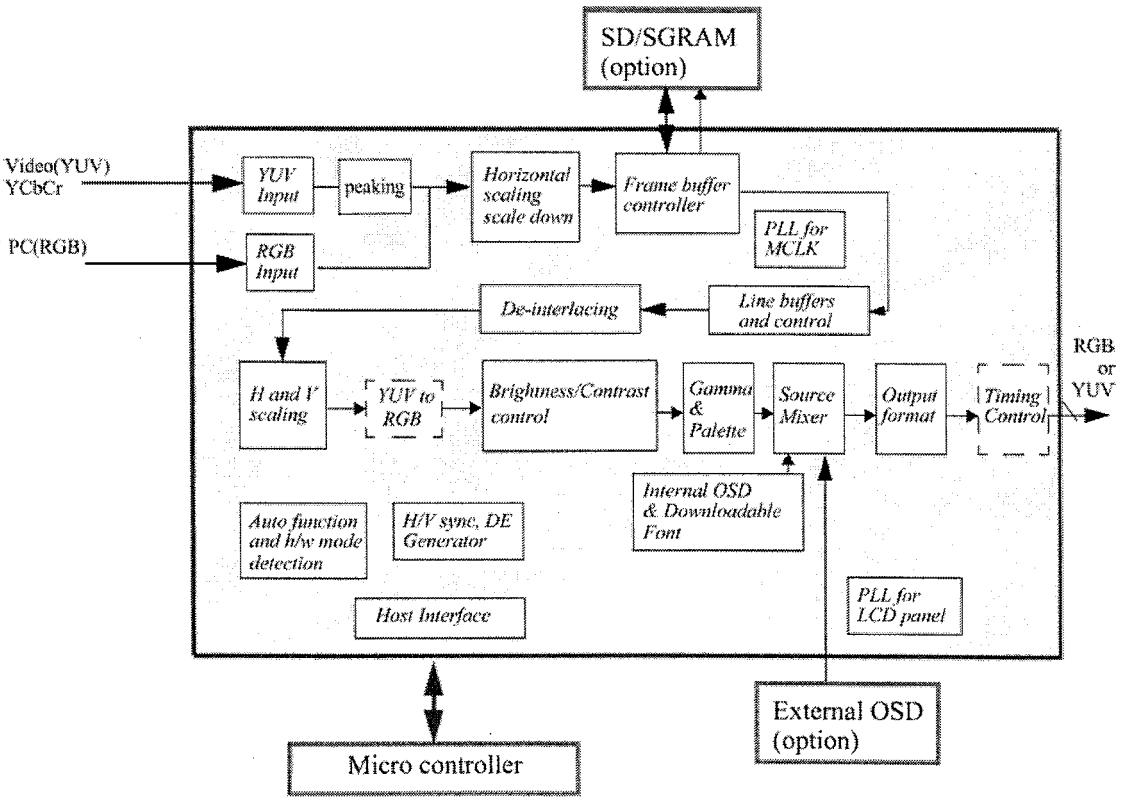


FIGURE 2. Block diagram of ZiproSX chips



2.9 Pinning of ZiproSX 160 pins

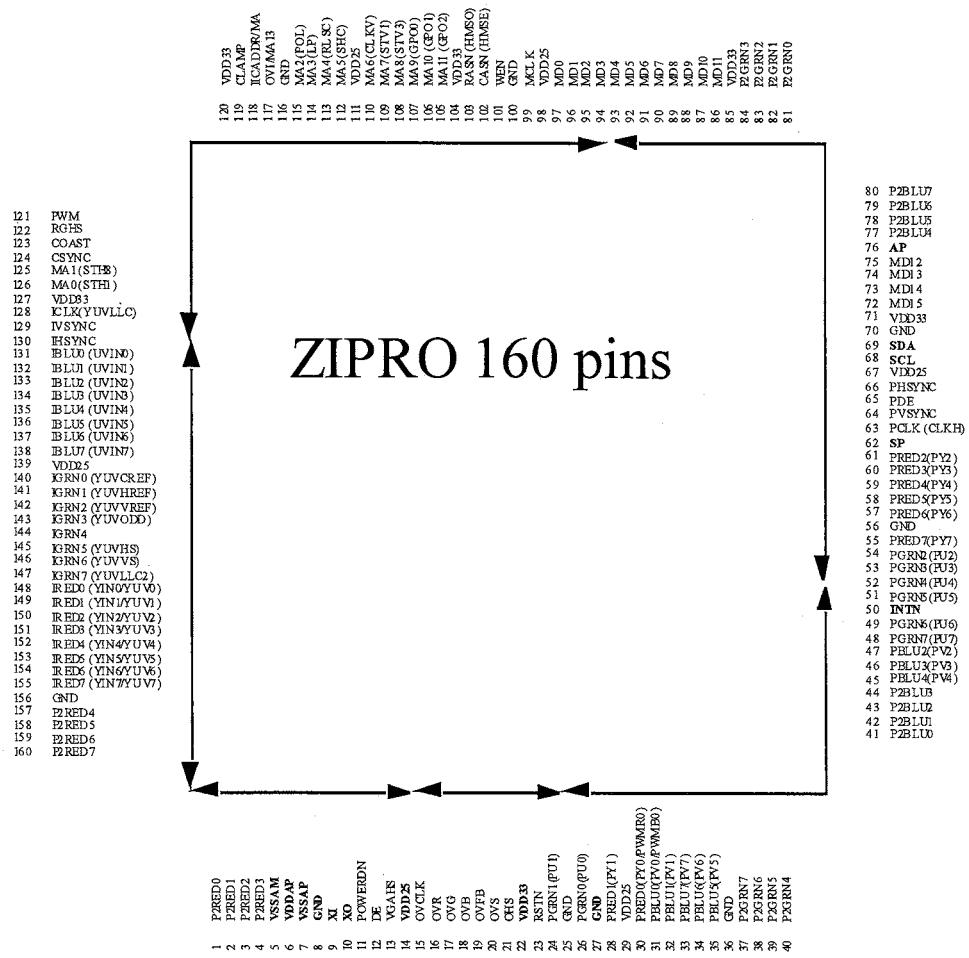


TABLE 1. Input Ports (RGB and YUV Data, 34 pins)

Pin #	I/O (drive)	Name	Description
128	I	ICLK(YUVLLC)	Clock for A port input (single/double pixel per clock).
129	I	IVSYNC	Vertical Sync of video A port.
130	I	IHSYNC	Horizontal Sync of video A port
155-148	I	IRED[7:0] /YIN[7:0]/YUV[7:0]/RGB12[11:4]	Red input data of video A port. The pin numbers are listed MSB to LSB. The RGB12bit uses this port and the MSB
147-140	I	IGRN[7:0]/RGB12[3:0]	Green input data of video A port. bit 7: YUVLLC2 bit 6: YUVVS bit 5: YUVHS bit 3: YUVODD (ODD or EVEN field) bit 2: YUVVREF bit 1: YUVHREF bit 0: YUVCREF
138-131	I	IBLU[7:0]/UV[7:0]	Blue input data of video A port.
123	O	COAST	COAST signal to ADC (regenerated VS).
122	O	RGHS	Regenerated HS
13	I	VGAHS	VGA input HS
12	I	DE	Display enable signal from digital flat panel interface. This signal should be tied to high if DE function is not use
124	I	CSYNC	Composite sync signal that includes HS and VS
119	O	CLAMP	Clamp pulse to ADC. This pin can also be programmed to FID, Cinema mode, or PWMR0.
121	O	PWM	Pulse width modulation output (NOTE: pin 23 is the VDD Zurac)

TABLE 2. Panel interface (or Display Port) RGB Data, 54 pins)

Pin #	I/O (drive)	Name	Description
63	O	PCLK (or PHCLK)	Display port A clock for panel (This clock is generated fro internal PLL)
65	O	PDE	Display enable (active area of display)
64	O	PVSYNC	Display Vertical Sync
66	O	PHSYNC	Display Horizontal Sync
55,57-61,28,30	O	PRED[7:0] /PY[7:0]/ODRED[7:0]	Display A port or Odd port of red data. The pin numbers are listed from MSB to LSB

Pin #	I/O (drive)	Name	Description
48-49,51-54,24,26	O	PGRN[7:0] /PU[7:0]/ODGRN[7:0]	Display A port or Odd port of green data.
33-35,45-47,32-31	O	PBLU[7:0] /PV[7:0]/ODBLU[7:0]	Display A port or Odd port of blue data
160-157,4-1	O	P2RED[7:0]/EVRED[7:0]	Display B port or Even port for red data.
37-40,84-81	O	P2GRN[7:0]/EVGRN[7:0]	Display B port or Even port green data
80-77,44-41	O	P2BLU[7:0]/EVBLU[7:0]	Display B port or Even port blue data
10	O	XO	Reference frequency output for internal oscillator
9	I	XI	Reference frequency input for internal oscillator (should be connected to a 14.31818MHz crystal)

TABLE 3. Host Interface Signals (6 pins)

Pin #	I/O (drive)	Name	Description
118	I/O	IICADDR	Serial I/F sub-address setting / Memory address bus bit 12
50	O	INTN	Interrupt to host (active low)
23	I	RSTN	Device reset (active low)
69	I/O	SDA	Serial I/F data in/out
68	I	SCL	Serial I/F clock
11	I	POWERDN	Power Down, 0: normal, 1:Powerdown

TABLE 4. Memory Control Port (Frame buffer) (32 pins)

Pin #	I/O (drive)	Name	Description
99	O	MCLK	Memory clock output
101	O	WEN	Memory write enable
102	O	CASN	Memory column address strobe
103	O	RASN	Memory row address strobe
72-75,86-97	I/O	MD[15:0]	Memory data bus
105-110,112-115,125,126	O	MA[11:0]	Memory address bus

TABLE 5. Overlay Port (External OSD) (8 pins)

Pin #	I/O (drive)	Name	Description
15	O	OVCLK	Clock for external overlay circuit.
16	I	OVR	Overlay color select R
17	I	OVG	Overlay color select G
18	I	OVB	Overlay color select B
117	I/O	OVI	Overlay intensity select / Memory address bus bit 13
19	I	OVFB	Overlay color enable
20	O	OVS	Overlay V sync signal
21	O	OHS	Overlay H sync signal

TABLE 6. Testing (2 pins)

Pin #	I/O (drive)	Name	Description
76	I	AP	Action pin for testing (should be grounded)
62	I	SP	Shift pin for testing (should be grounded)

FIGURE 3. Timing Control (48+18 shared pins)

Pin #	I/O	Dr (mA)	Pin name of t0947(ZiproSX)	Pin name of t0949(ZiproTC2)	Description
-	O	4	PRED[7:0], PGRN[7:0], PBLU[7:0]	ODRED[7:0], ODGRN[7:0], ODBLU[7:0]	Odd RGB pixel data (24 pins) Note: The 1st pixel is at the ODD bus in ZiproTC2.
-	O	4	P2RED[7:0], P2GRN[7:0], P2BLU[7:0]	EVRED[7:0], EVGRN[7:0], EVBLU[7:0]	Even RGB pixel data (24 pins) Note: The 2nd pixel is at the EVEN bus in ZiproTC
63	O	16	PCLK	CLKH	Clock for source driver IC
126	O	4	MA0	STH1	Start pulse for source driver IC (S1 to S8)
125	O	4	MA1	STH8	Start pulse for source driver IC (S8 to S1)
115	O	4	MA2	POL	Polarity for source driver IC
114	O	4	MA3	LP	Latch pulse for source driver IC
103	O	4	RASN	HMSO	Data inversion control for odd pixel bus (if more than half signals in the bus change state, this will be set.)
102	O	4	CASN	HMSE	Data inversion control for even pixel bus
113	O	4	MA4	RLSC	R/L indication for source driver IC

Pin #	I/O	Dr (mA)	Pin name of t0947(ZiproSX)	Pin name of t0949(ZiproTC2)	Description
112	O	4	MA5	SHC	decode control for TI driver IC
110	O	4	MA6	CLKV	Clock for gate driver IC
109	O	4	MA7	STV1	Start pulse for gate driver IC (G1 to G3)
108	O	4	MA8	STV3	Start pulse for gate driver IC (G3 to G1)
107	O	4	MA9	GPO0	Programmable general purpose output 0
106	O	4	MA10	GPO1	Programmable general purpose output 1
105	O	4	MA11	GPO2	Programmable general purpose output 2
66	O	4	PHS	PHS	Panel H sync output signal
64	O	4	PVS	PVS	Panel V sync output signal
65	O	4	PDE	PDE	Panel display enable output signal

TABLE 7. Power and Ground Signals (24 pins include 14 VDD and 10 GND pins)

Pin #	V	Name	Description
14,29,67,98,111,139	2.5	VDD25	Digital power supply (for core cells)
22,71,85,104,120,127	3.3	VDD33	Digital power supply (for I/O cells)
8,25,**27**,36,56,70,100,116,1	0	GND	Ground
5	0	VSSAM	Ground pin for MCLK PLL
6	2.5	VDDAP	Power pin for PCLK and MCLK PLL
7	0	VSSAP	Ground pin for PCLK PLL

Pin no.	Pin name	Pin no.	Pin name
1	P2RED0 **(EVRED0)**	41	P2BLU0 **(EVBLU0)**
2	P2RED1 **(EVRED1)**	42	P2BLU1 **(EVBLU1)**
3	P2RED2 **(EVRED2)**	43	P2BLU2 **(EVBLU2)**
4	P2RED3 **(EVRED3)**	44	P2BLU3 **(EVBLU3)**
5	**VSSAM**	45	PBLU4(PV4) **(ODBLU4)**
6	**VDDAP**	46	PBLU3(PV3) **(ODBLU3)**
7	**VSSAP**	47	PBLU2(PV2) **(ODBLU2)**
8	**GND**	48	PGRN1(PU1) **(ODGRN1)**
9	**XI**	49	PGRN0(PU0) **(ODGRN0)**
10	**XO**	50	**INTN**
11	POWERDN	51	PGRN5(PU5) **(ODGRN5)**
12	DE	52	PGRN4(PU4) **(ODGRN4)**
13	VGAHS	53	PGRN3(PU3) **(ODGRN3)**
14	**VDD25**	54	PGRN2(PU2) **(ODGRN2)**
15	OVCLK	55	PRED7(PY7) **(ODRED7)**

Pin no.	Pin name	Pin no.	Pin name
16	OVR	56	GND
17	OVG	57	PRED6(PY6) **(ODRED6)**
18	OVB	58	PRED5(PY5) **(ODRED5)**
19	OVFB	59	PRED4(PY4) **(ODRED4)**
20	OVS	60	PRED3(PY3) **(ODRED3)**
21	OHS	61	PRED2(PY2) **(ODRED2)**
22	**VDD33**	62	**SP**
23	RSTN	63	PCLK **(CLKH)**
24	PGRN1 **(PU1/ODGRN1)**	64	PVSYNC **(PVS)**
25	GND	65	PDE **(PDE)**
26	PGRN0 **(PU0/ODGRN0)**	66	PHSYNC **(PHS)**
27	**GND**	67	VDD25
28	PRED1 **(PY1/ODRED1)**	68	**SCL**
29	VDD25	69	**SDA**
30	PRED0 (PY0/PWMR0)	70	GND
	(ODRED0)		
31	PBLU0 (PV0/PWMB0)	71	VDD33
	(ODBLU0)		
32	PBLU1 **(PV1/ODBLU1)**	72	MD15
33	PBLU7 (PV7) **(ODBLU7)**	73	MD14
34	PBLU6 (PV6) **(ODBLU6)**	74	MD13
35	PBLU5 (PV5) **(ODBLU5)**	75	MD12
36	GND	76	**AP**
37	P2GRN7 **(EVGRN7)**	77	P2BLU4 **(EVBLU4)**
38	P2GEN6	78	P2BLU5 **(EVBLU5)**
39	P2GRN5 **(EVGRN5)**	79	P2BLU6 **(EVBLU6)**
40	P2GEN4	80	P2BLU7 **(EVBLU7)**

Pin no.	Pin name	Pin no.	Pin name
81	P2GRN0 **(EVGRN0)**	121	PWM
82	P2GRN1 **(EVGRN1)**	122	RGHS
83	P2GRN2 **(EVGRN2)**	123	COAST
84	P2GRN3 **(EVGRN3)**	124	CSYNC
85	VDD33	125	MA1(**STH8**)
86	MD11	126	MA0(**STH1**)
87	MD10	127	VDD33
88	MD9	128	ICLK(YUVLLC)
89	MD8	129	IVSYNC

90	MD7	130	IHSYNC
91	MD6	131	IBLU0(UVIN0)
92	MD5	132	IBLU1(UVIN1)
93	MD4	133	IBLU2(UVIN2)
94	MD3	134	IBLU3(UVIN3)
95	MD2	135	IBLU4(UVIN4)
96	MD1	136	IBLU5(UVIN5)
97	MD0	137	IBLU6(UVIN6)
98	VDD25	138	IBLU7(UVIN7)
99	MCLK	139	VDD25
100	GND	140	IGRN0(YUVCREF)
101	WEN	141	IGRN1(YUVVREF)
102	CASN **(HMSE)**	142	IGRN2(YUVVREF)
103	RASN **(HMSO)**	143	IGRN3(YUVODD)
104	VDD33	144	IGRN4
105	MA11 **(GPO2)**	145	IGRN5(YUVHS)
106	MA10 **(GPO1)**	146	IGRN6(YUVVS)
107	MA9 **(GPO0)**	147	IGRN7(YUVLLC2)
108	MA8 **(STV3)**	148	IRED0(YIN0/YUV0)
109	MA7 **(STV1)**	149	IRED1(YIN1/YUV1)
110	MA6 **(CLKV)**	150	IRED2(YIN2/YUV2)
111	VDD25	151	IRED3(YIN3/YUV3)
112	MA5 **(SHC)**	152	IRED4(YIN4/YUV4)
113	MA4 **(RLSC)**	153	IRED5(YIN5/YUV5)
114	MA3 **(LP)**	154	IRED6(YIN6/YUV6)
115	MA2 **(POL)**	155	IRED7(YIN7/YUV7)
116	GND	156	GND
117	OVI(MA13)	157	P2RED4
118	IICADDR/MA12	158	P2RED5
119	CLAMP	159	P2RED6
120	VDD33	160	P2RED7

2.10 Pinning of ZiproSX 128 pins

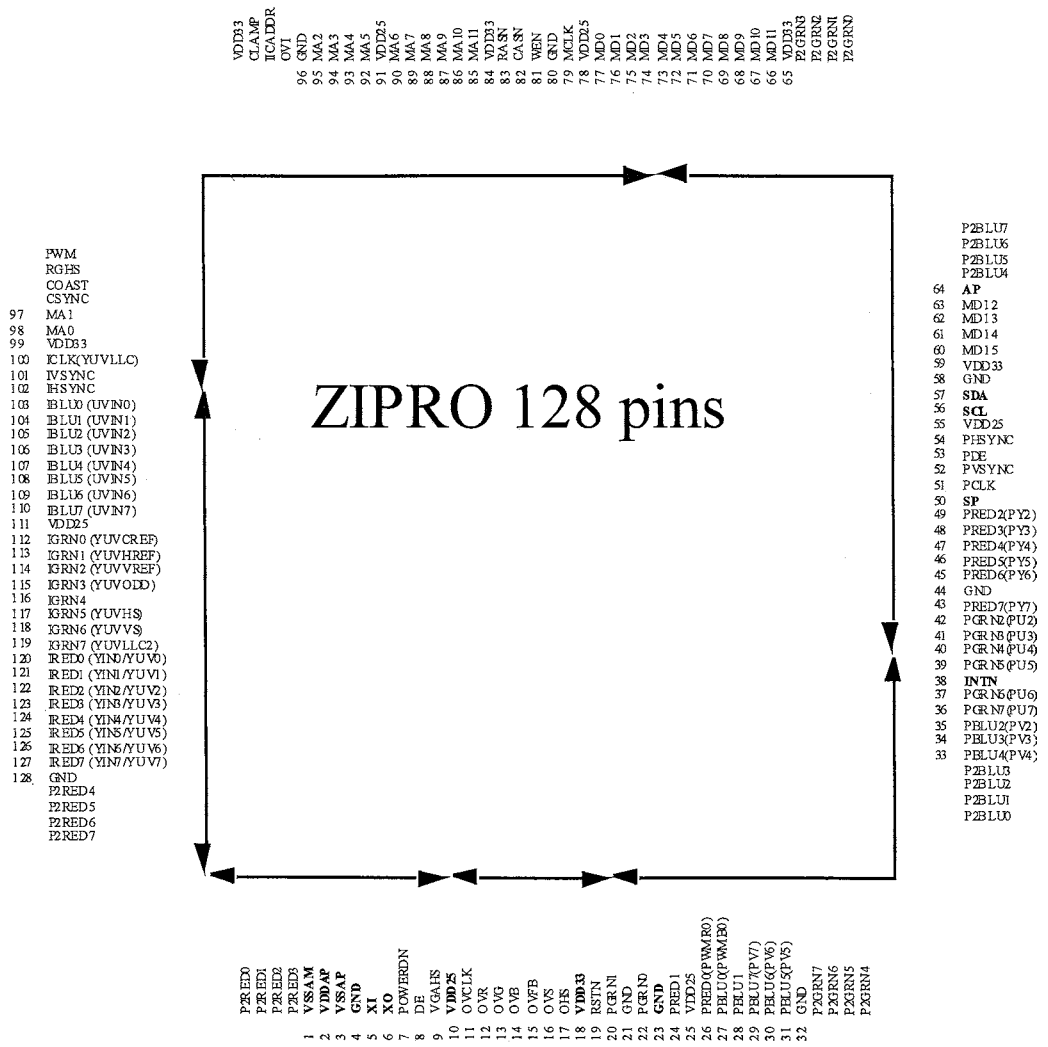


TABLE 8. Input Ports (RGB and YUV Data, 34 pins)

Pin #	I/O (drive)	Name	Description
100	I	ICLK(YUVLLC)	Clock for A port input (single/double pixel per clock).
101	I	IVSYNC	Vertical Sync of video A port.
102	I	IHSYNC	Horizontal Sync of video A port
127-120	I	IRED[7:0] /YIN[7:]/YUV[7:0]/RGB12[11:4]	Red input data of video A port. The pin numbers are listed from MSB to LSB. The RGB12bit uses this port and the MSB of IGRN port.
119-112	I	IGRN[7:0]/RGB12[3:0]	Green input data of video A port. bit 7: YUVLLC2 bit 6: YUVVS bit 5: YUVHS bit 3: YUVODD (ODD or EVEN field) bit 2: YUVVREF bit 1: YUVHREF bit 0: YUVCREF
110-103	I	IBLU[7:0]/UV[7:0]	Blue input data of video A port
9	I	VGAHS	VGA input HS
8	I	DE	Display enable signal from digital flat panel interface. This signal should be tied to high if DE function is not used

TABLE 9. Panel interface (or Display Port) (RGB Data, 54 pins)

Pin #	I/O (drive)	Name	Description
51	O	PCLK	Display port A clock for panel (capability is 8 mA) (This clock is generated from internal PLL)
53	O	PDE	Display enable (active area of display)
52	O	PVSYNC	Display Vertical Sync
54	O	PHSYNC	Display Horizontal Sync
43,45-49,24,26	O	PRED[7:0] /PY[7:0]	Display A port red data.
36-37,39-42,20,22	O	PGRN[7:0]/PU[7:0]	Display A port green data. The pin numbers are listed from MSB to LSB
29-31,33-35,28-27	O	PBLU[7:0]/PV[7:0]	Display A port blue data
6	O	XO	Reference frequency output for internal oscillator
5	I	XI	Reference frequency input for internal oscillator (should be connected to a 14.31818MHz crystal)

TABLE 10. Host Interface Signals (6 pins)

Pin #	I/O	Name	Description
38	O	INTN	Interrupt to host (active low)
19	I	RSTN	Device reset (active low)
57	I/O	SDA	Serial I/F data in/out
56	I	SCL	Serial I/F clock
7	I	POWERDN	Power Down, 0: normal, 1:Powerdown

TABLE 11. Memory Control Port (Frame buffer) (32 pins)

Pin #	I/O	Name	Description
79	O	MCLK	Memory clock output
81	I	WEN	Memory write enable
82	I	CASN	Memory column address strobe
83	I	RASN	Memory row address strobe
60-63,66-77	I	MD[15:0]	Memory data bus
85-90,92-95,97-98	I	MA[11:0]	Memory address bus

TABLE 12. Overlay Port (External OSD) (8 pins)

Pin #	I/O	Name	Description
11	O	OVCLK	Clock for external overlay circuit.
12	I	OVR	Overlay color select R
13	I	OVG	Overlay color select G
14	I	OVB	Overlay color select B
15	I	OVFB	Overlay color enable
16	O	OVS	Overlay V sync signal
17	O	OHS	Overlay H sync signal

TABLE 13. Testing (2 pins)

Pin #	I/O	Name	Description
64	I	AP	Action pin for testing (should be grounded)
50	I	SP	Shift pin for testing (should be grounded)

TABLE 14. Power and Ground Signals (23 pins include 13 VDD and 10 GND pins)

Pin #	I/O	Name	Description
10,25,55,78,91,111	2.5	VDD25	Digital power supply (for core cells)
18,59,65,84,99	3.3	VDD33	Digital power supply (for I/O cells)
4,21,**23**,32,44,58,80,96,1	0	GND	Ground
1	0	VSSAM	Ground pin for MCLK PLL
2	2.5	VDDAP	Power pin for PCLK and MCLK PLL
3	0	VSSAP	Ground pin for PCLK PLL

Pin no.	Pin name	Pin no.	Pin name
1	**VVSAM**	33	PBLU4(PV4)
2	**VDDAP**	34	PBLU3(PV3)
3	**VSSAP**	35	PBLU2(PV2)
4	**GND**	36	PGRN7(PU7)
5	**XI**	37	PGRN6(PU6)
6	**XO**	38	**INTN**
7	POWERDN	39	PGRN5(PU5)
8	DE	40	PGRN4(PU4)
9	VGAHS	41	PGRN3(PU3)
10	**VDD25**	42	PGRN2(PU2)
11	OVCLK	43	PRED7(PY7)
12	OVR	44	GND
13	OVG	45	PRED6(PY6)
14	OVB	46	PRED5(PY5)
15	OVFB	47	PRED4(PY4)
16	OVS	48	PRED3(PY3)
17	OHS	49	PRED2(PY2)
18	**VDD33**	50	**SP**
19	RSTN	51	PCLK
20	PGRN1	52	PVSYNC
21	GND	53	PDE
22	PGRN0	54	PHSYNC
23	**GDN**	55	VDD25
24	PRED1	56	**SCL**
25	VDD25	57	**SDA**
26	PRED0(PWMR0)	58	GND
27	PBLU0(PWMB0)	59	VDD33
28	PBLU1	60	MD15
29	PBLU7(PV7)	61	MD14
30	PBLU6(PV6)	62	MD13
31	PBLU5(PV5)	63	MD12
32	GND	64	**AP**

Pin no.	Pin name	Pin no.	Pin name
65	VDD33	97	MA1
66	MD11	98	MA0
67	MD10	99	VDD33
68	MD9	100	ICLK
69	MD8	101	IVSYNC
70	MD7	102	IHSYNC
71	MD6	103	IBLU0(UVIN0)
72	MD5	104	IBLU1(UVIN1)
73	MD4	105	IBLU2(UVIN2)
74	MD3	106	IBLU3(UVIN3)
75	MD2	107	IBLU4(UVIN4)
76	MD1	108	IBLU5(UVIN5)
77	MD0	109	IBLU6(UVIN6)
78	VDD25	110	IBLU7(UVIN7)
79	MCLK	111	VDD25
80	GND	112	IGRN0(YUVCREF)
81	WEN	113	IGRN1(YUVVREF)
82	CASN	114	IGRN2(YUVVREF)
83	RASN	115	IGRN3(YUVODD)
84	VDD33	116	IGRN4
85	MA11	117	IGRN5(YUVHS)
86	MA10	118	IGRN6(YUVVS)
87	MA9	119	IGRN7(YUVLLC2)
88	MA8	120	IRED0(YIN0/YUV0)
89	MA7	121	IRED1(YIN1/YUV1)
90	MA6	122	IRED2(YIN2/YUV2)
91	VDD25	123	IRED3(YIN3/YUV3)
92	MA5	124	IRED4(YIN4/YUV4)
93	MA4	125	IRED5(YIN5/YUV5)
94	MA3	126	IRED6(YIN6/YUV6)
95	MA2	127	IRED7(YIN7/YUV7)
96	GND	128	GND

3.0 CHARACTERISTICS

3.1 Recommended Operating Conditions

Item	Value
Operating voltage	2.5V and 3.3V plus/minus 10%
Operating chassis temperature	0℃ to 80℃
Total power dissipation	Max. 0.64 W (XGA LCD panel @ 85Hz)

3.2 DC CHARACTERISTICS

VDD3 = 3.0 to 3.6V; VDD2 = 2.25 to 2.75V; VDDAP = 2.4 to 2.6V; Tamb= 25 C; unless otherwise specified.

SYMBOL	PARAMETER	Remark	MIN.	TYP.	MAX.	UNIT
Powers						
VDD3	I/O digital supply voltage		3.0	3.3	3.6	V
VDD2	core digital supply voltage		2.25	2.5	2.75	V
VDDAP	PLL A+D supply voltage		2.4	2.5	2.6	V
I_{DD3}	I/O digital supply current		-	-	80	mA
I_{DD2}	core digital supply current		-	-	150	mA
Digital inputs						
$VIL_{(SDA, SCL)}$	input low level of SDA, SCL		-0.5	-	0.3*VDD3	V
$VIH_{(SDA, SCL)}$	input high level of SDA, SC L		0.7*VDD3	-	5.0+0.5	V
$VIL_{(IA/BCLK)}$	input low level of clock pins		-0.5	-	0.6	V
$VIH_{(IA/BCLK)}$	input high level of clock pins		2.2	-	5.0+0.5	V
$VIL_{(all\ other)}$	input low level of other inputs		-0.5	-	0.8	V
$VIH_{(all\ other)}$	input high level of other inputs		2.0	-	5.0+0.5	V
ILI	input leakage current		-	-	10.0	uA
Digital outputs						
$VOL_{(SDA)}$	output low level @ SDA	IOL=3mA	-	-	0.4	V
$VOL_{(all\ other)}$	output low level of all other		-	-	0.4	V
$VOH_{(all\ other)}$	output high level of all other		2.4	-	-	V

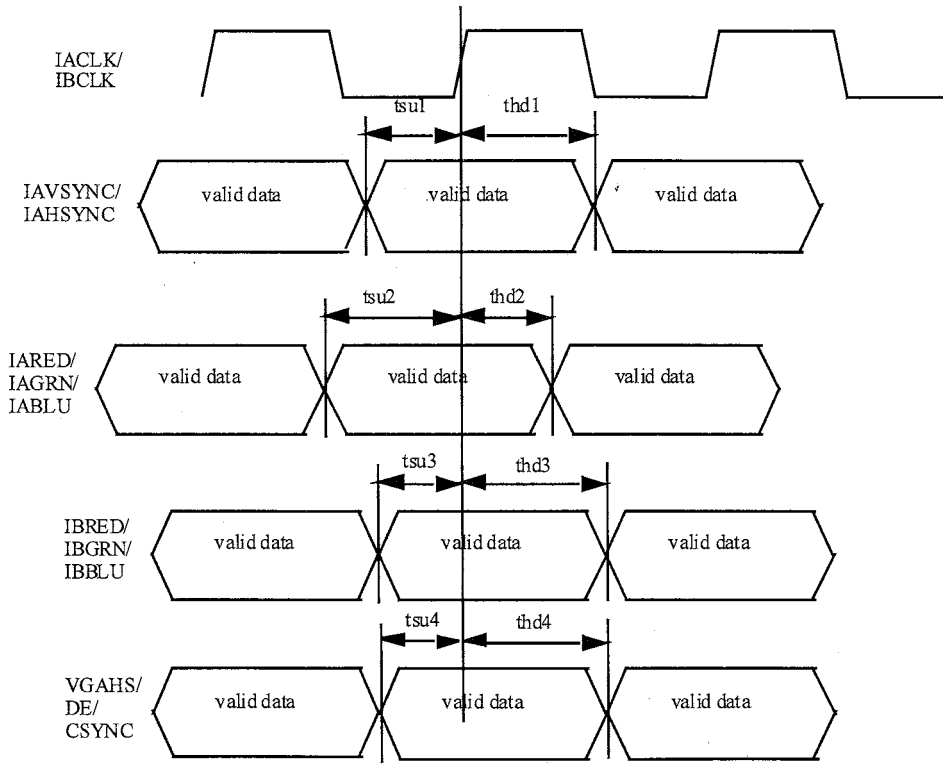
3.3 AC CHARACTERISTICS

All timing is measured at 1.5V logic switching threshold and VDD3 = 3.3V; VDD2 = 2.5V; VDDAP = 2.5V; T_{amb}= 25^{o}C; unless otherwise specified.

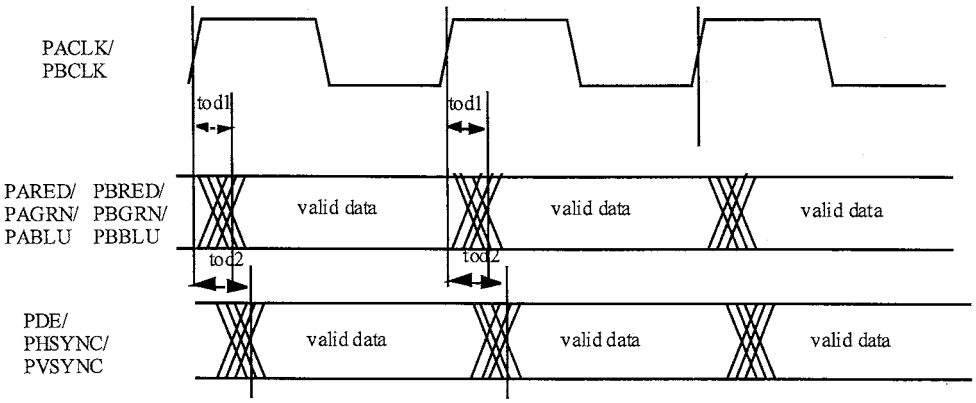
SYMBOL	PARAMETER	min. setup time	min. hold time	UNIT
Input signals (RGB / YUV data and overlay ports)				
tsu1/thd1	IAVSYNC/IAHSYNC setup/hold time	3.0	1.0	ns

tsu2/thd2	IAR/IAG/IAB input data setup/hold time	3.0	1.0	ns
tsu3/thd3	IBR/IBG/IBB input data setup/hold time	3.0	1.0	ns
tsu4/thd4	control signal (VGAHS/DE/CSYNC) setup/hold time	3.0	1.0	ns
tsu5/thd5	Overlay inputs (OVR/G/B/I/FB) setup/hold time	1.0	3.4	ns
Output signals		**max. delay time**		
tod1	pixel data output delay (PAR/G/B, PBR/G/B)	4.5		ns
tod2	control signal (PDE, PHS/PVS) output delay	5.0		ns

INPUT TIMINGS



OUTPUT TIMINGS



4.0 FUNCTIONAL DESCRIPTION OF BLOCKS

4.1 YUV input port

The YUV input port supports interlaced video streams and provides connection to most common decoder ICs.

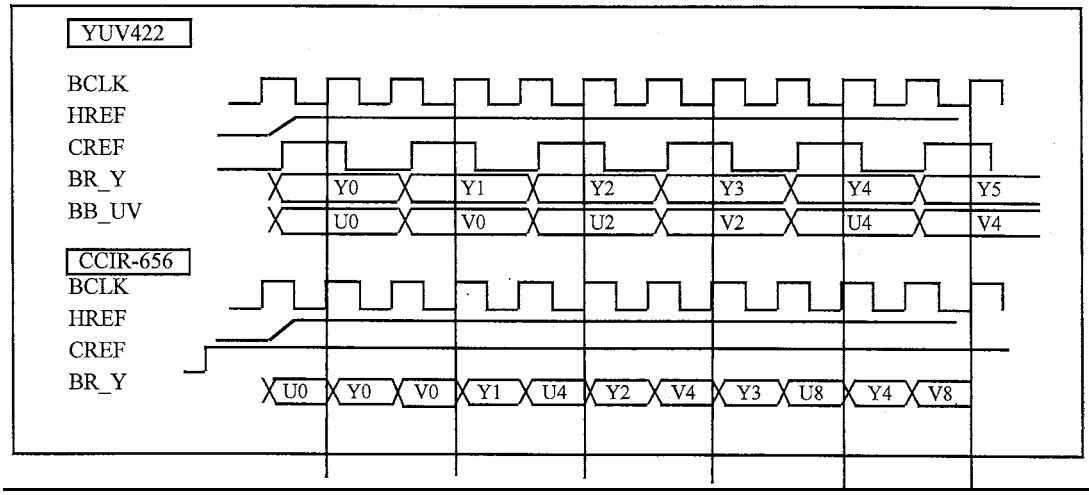
This chip supports 8-bit YUV 4:2:2 (CCIR 656), 16-bit YUV 4:2:2 video input. Each input format can be binary offset or 2's complement.

The YUV input formats are tabulated below. The selection of YUV or RGB inputs are activated by the setting of YUVF (bit 4 of INCTR1 or 02 hex) bit.

TABLE 15.

Signal	16-bit 4:2:2		8-bit 4:2:2 (CCIR-656)			
YIN7	Y07	Y17	U07	Y07	V07	Y17
YIN6	Y06	Y16	U06	Y06	V06	Y16
YIN5	Y05	Y15	U05	Y05	V05	Y15
YIN4	Y04	Y14	U04	Y04	V04	Y14
YIN3	Y03	Y13	U03	Y03	V03	Y13
YIN2	Y02	Y12	U02	Y02	V02	Y12
YIN1	Y01	Y11	U01	Y01	V01	Y11
YIN0	Y00	Y10	U00	Y00	V00	Y10
UVIN7	U07	V07				
UVIN6	U06	V06				
UVIN5	U05	V05				
UVIN4	U04	V04				
UVIN3	U03	V03				
UVIN2	U02	V02				
UVIN1	U01	V01				
UVIN0	U00	V00				

FIGURE 4. Input YUV format & timing



4.2 JPEG-write input port

The JPEG-write input port is implemented to display a picture decoded by an external JPEG decoder. The basic timing for JPEG-write is shown below: The input data of JPEG write is in 8-bit YUV422 or U0-Y0-V0-Y1 format.

There are three operation mode of JPEG write procedure. Legacy mode is compatible with Zipro (t0944); Horizontal and Vertical auto-incremental mode are proposed for more efficient JPEG programming interface.

4.3 Input/output window definition

This section describes the input window. The signals IH_PULW, IH_ASTART and IH_TOTAL count from IHS falling edge. If IH_ASTART= n and IH_AWIDTH = w, then the first and the last active data are D_{n+1} and D_{n+w} respectively. If IV_ASTART=n and IV_ACTIVE = w, then the fist active line is Ln and last active line is L_{n+w-1}.

FIGURE 5. INPUT WINDOW PARAMETER:

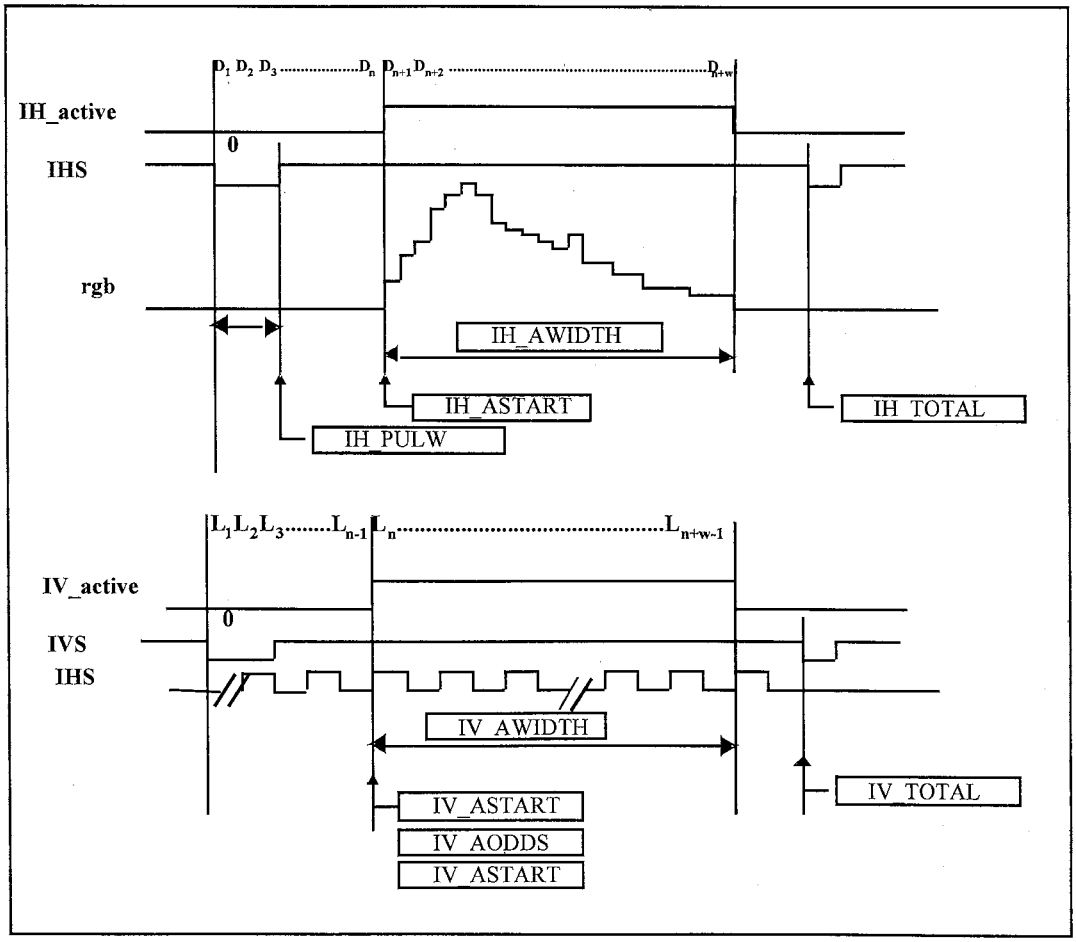
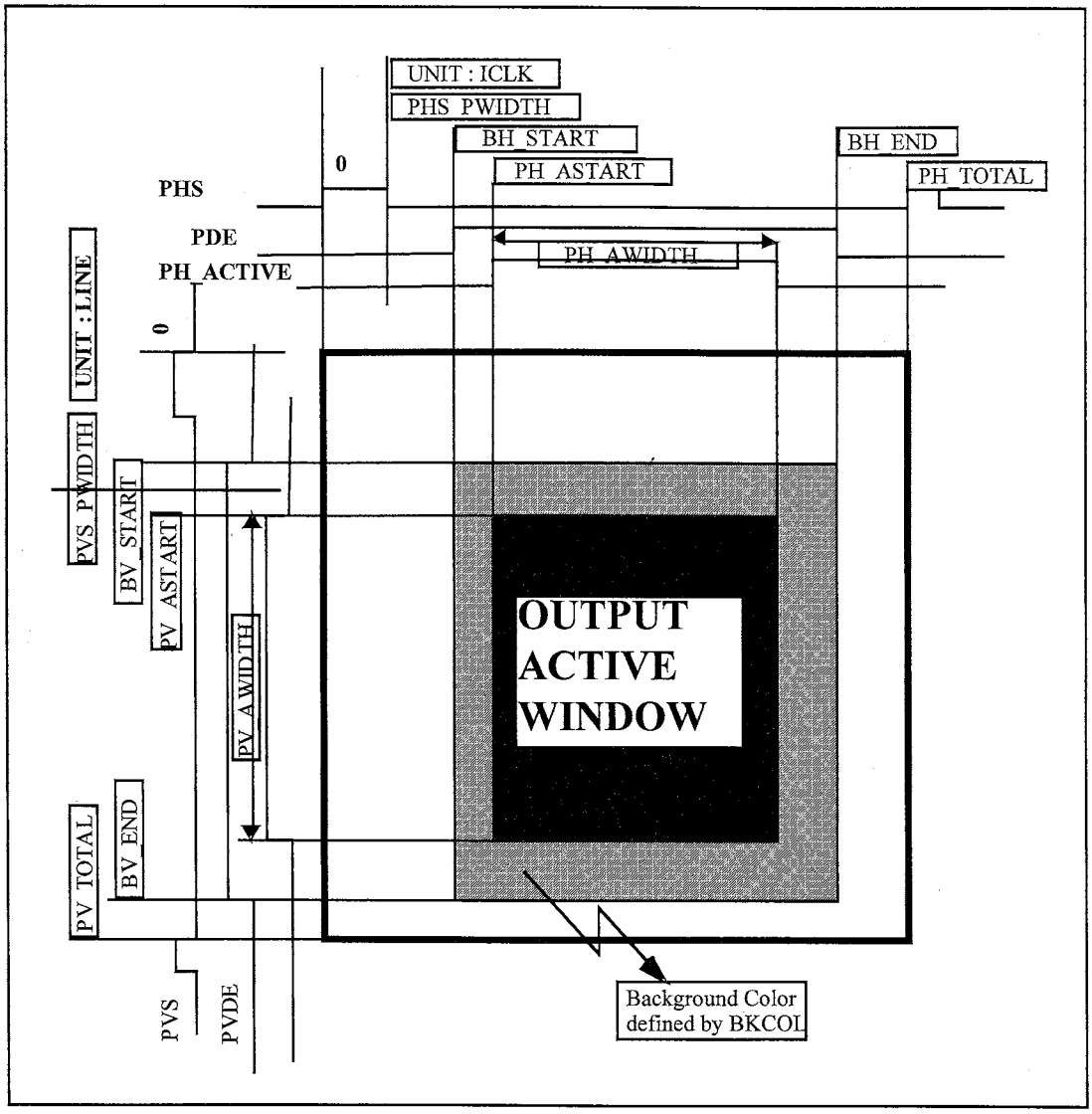
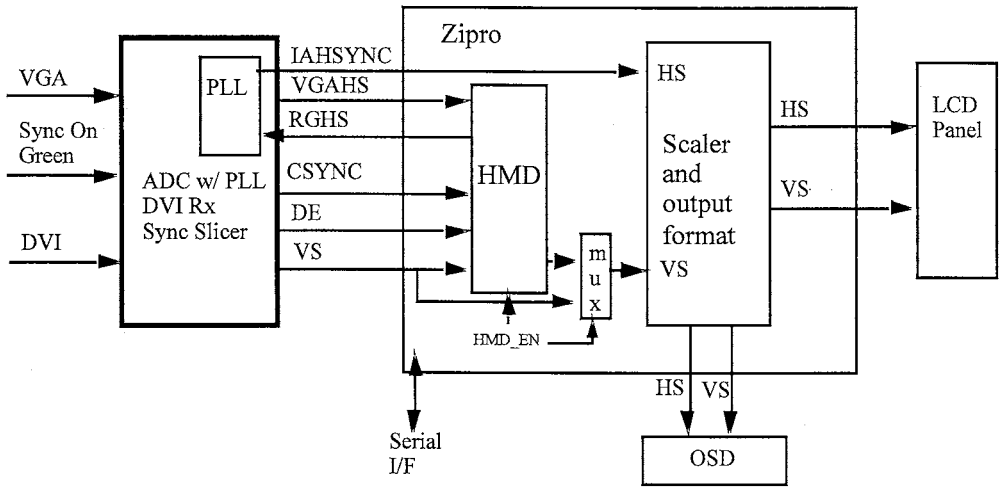


FIGURE 6. Output Window parameters.



4.4 Hardware Mode Detection (HMD)

Hardware mode detection detects the presences and frequencies of HS, VS, and DE.



4.5 Color adjust and color space convert (matrix)

The ZiproSX and ZiproTC2 chip accepts either RGB or YUV and feeds to display devices in RGB format.

The RGB adjustments are

Rout = R*contrast + brightness

Gout = G*contrast + brightness

Bout = B*contrast + brightness

Note that the contrast control uses a 8-bit signal to set a multiply value from 2 to 0 (in fact, the 256 choices are 255/128, 254/128, ..., 128/128, .., 1/128, 0). The brightness correction uses a 8-bit signal to set an offset value from 127 to -128 (the 256 choices are 127, 126, ..., 1, 0, -1, ..., -127, -128). The control signals BRIGHTNESS[7:0] and CONTRAST[7:0] are programmable via serial interface.

The formula to set CONTRAST[7:0] value is ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0]. For brightness control, the signal BRIGHTNESS[7:0] is interpreted as a 2s complement value. These settings are tabulated as **TABLE 17.**

Contrast correction for MSB=0					
contrast[7:0]	7f(hex)	7e	02	01	00
multiply value	255/128	254/128	130/128	129/128	128/128
Contrast correction for MSB=1					
contrast[7:0]	ff(hex)	fe	82	81	80
multiply value	127/128	126/128	2/128	1/128	0/128

Brightness correction for MSB=0						
brightness[7:0]	7f(hex)	7e	7d	02	01	00
offset value	127	126	125 .	2	1	0
Brightness correction for MSB=1						
brightness[7:0]	ff(hex)	fe	fd	82	81	80
offset value	-1	-2	-3	-126	-127	-128

The block diagram is depicted as follows:

FIGURE 7. Function of contrast followed by brightness control for each RGB.

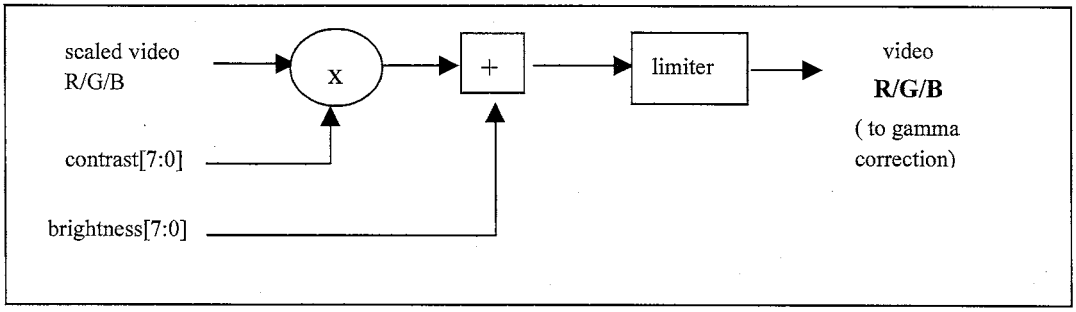
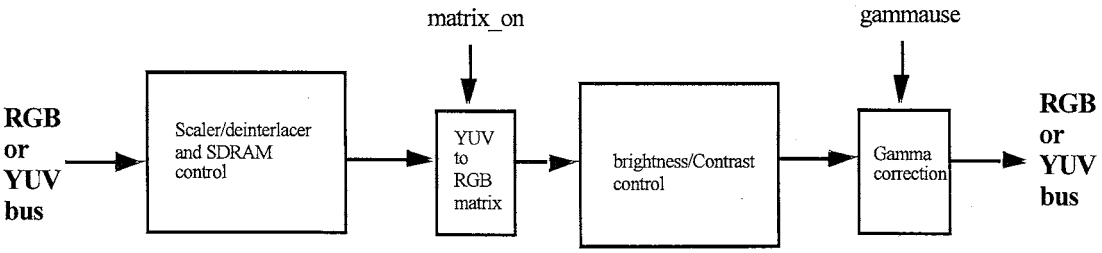


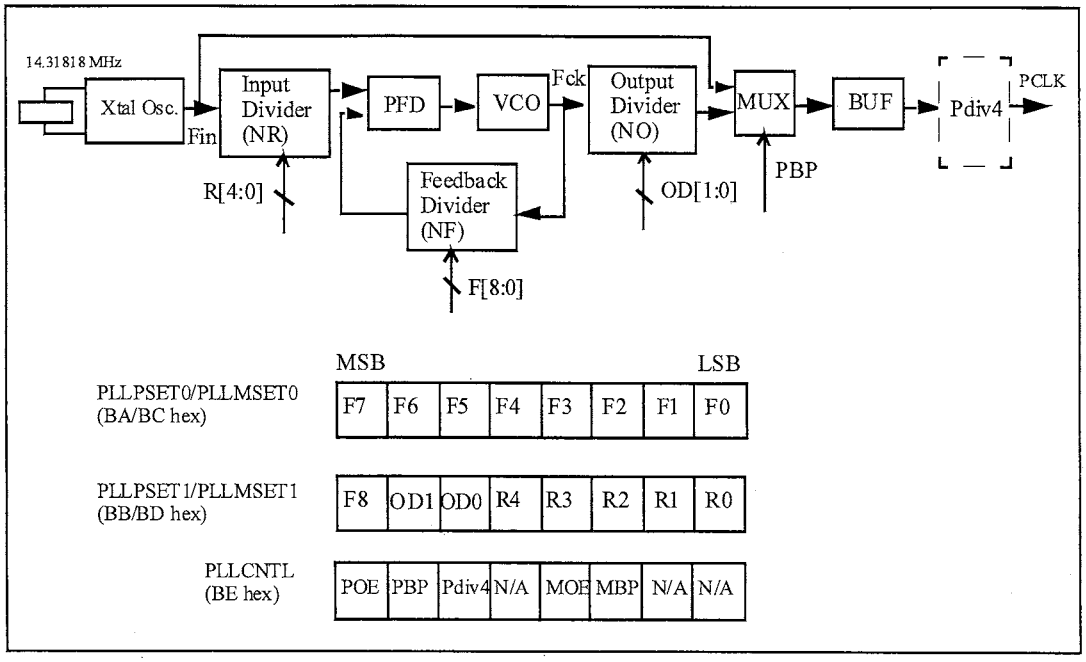
FIGURE 8. Data path for RGB/YUV in and RGB/YUV out



4.6 Clock system

t0947/t0949 chips have two PLL for PCLK and MLCK generation. PCLK is used for display panel clocking and MCLK for SD/SGRAM memory interface. These PLLs synthesize clocks via the 2-wire serial bus programming. The registers and block diagram are depicted as follows:

FIGURE 9. MPLL/PPLL Block diagram and control registers:



PLL program parameter				
PLLPSET0 FI(7 downto 0)	BA	4F	W	F7(MSB), F6, F5, F4, F3, F2, F1, F0 (LSB) The 8 LSB of feedback 9-bit divider The default value will set the PCLK to 65MHz
PLLPSET1	BB	47	W	F8(MSB), OD1, OD0, R4, R3, R2, R1, R0 (LSB)
FI(8) & ODI (1 down to 0) & RI(4 down to 0)				F8 is the MSB of feedback 9-bit divider, OD0 (MSB) and OD1 (LSB) are the control pins for output divider, and R4 to R0 are the pins for input 5-bit divider
PLLMSET0 FI(7 down to 0)	BC	7C	W	F7(MSB), F6, F5, F4, F3, F2, F1, F0 (LSB) The 8 LSB of feedback 9-bit divider The default value will set the MCLK to 100 MHz
PLLMSET1 FI(8) & ODI (1 down to 0) & RI(4 down to 0)	BD	47	W	F8(MSB), OD1, OD0, R4, R3, R2, R1, R0 (LSB) F8 is the MSB of feedback 9-bit divider, OD0 (MS and OD1 (LSB) are the control pins for output divider, and R4 to R0 are the pins for input 5-bit divider.

PLLCNTL Output enable and bypass control for Pclk and Mclk PLL.	BE	00	W	POE(MSB), PBP, Pdiv4, xx, MOE, MBP,xx, BACLK_SEL (LSB) where POE is the freq Output Enable of Pclk PLL (default 0), PBP is the ByPass control of Pclk PLL (default 0), and MOE/MBP are for Mclk PLL, xx is do not care. PLL will go to power down mode as the external POWERDN pin activated. Pdiv4 is used to further divide the Pclk frequency by the factor of 4 or not.

1. The frequency derived from the PLL frequency synthesizer is formulated as follows:
   PCLK/MCLK = Fin * NF/(NR*NO).
   Where Fck = Fin*NF/NR, the output freq of VCO, should be in the range of 80 MHz to 200 MHz. The freq of PCLK can be modified by programming the register of NF, NR, and OD. The values of the divider should be set by subtracting the actual value by 2, i.e. if divided by 8 is what we want, then the binary values of the input control register should be set to 6 (e.g. NF is 000000110). The output divider (NO) control register is set by the following.
2. The bit BP (bypass) will be set to 1, if PLL is being tested, otherwise reset for normal PLL function.

TABLE 18.

Output Divider	**Divided by**
OD1=0 OD0=0	NO=1
OD1=0 OD0=1	NO=2
OD1=1 OD0=0	NO=2
OD1=1 OD0=1	NO=4

For example, if we want to get a 100 MHz output freq clock and Fin=14.31818 MHz, we need to set NF/NR = 140/10,and OD=2. In a sense, NF=010001010(bin), NR=01000, and OD=10.
Another example, if we want to get a 65 MHz output freq clock for XGA LCD panel and Fin=14.31818 MHz, we need to set NF/NR = 227/25, and OD=2. In a sense, NF=227-2=e1(hex), NR=25-2=17(hex), and OD=10(bin). Therefore, we need to program the register PLLPSET0 (BA) with a value e1(hex) and PLLPSET0 (BB) with 57.
Pclk can be further divided by the factor of 4 using Pdiv4.
MCLK can be turn off by program the register FBC_BYPASS (FBCTR2[6]) to “1”

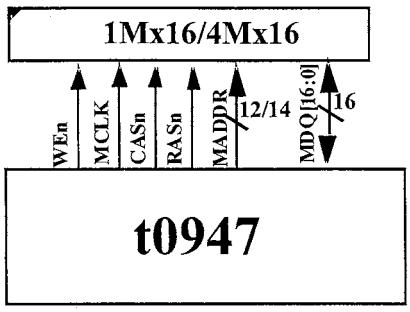
4.7 Memory Interface

The ZiproSX(t0947) chips perform frame rate conversion (FRC) by replicating or dropping the input frames using the external SDRAM as the frame buffers. The major features are:

- Double-buffer mechanism is used to prevent the frame tearing.
- The data path width to the external SDRAM is 16 bits.
- Programmable sub-image store/display for cropping and panning.
- Programmable top/bottom and left/right reversal for scan sequence flipping.
- Full screen freeze.
- De-interlacing scheme is used for preventing the motion artifacts as in the video.

The block diagram of the memory interface is the following:

FIGURE 10. Block Diagram of the Memory I/F



ZiproSX chip, t0947, supports one 1Mbx16 or one 4Mx16 SDRAM access. In a word, the frame buffer data path is 16-bit. Speed grades of 83-125 MHz are suggested. The data compression of 24-bit to 16-bit is also supported for reducing the access bandwidth. ZiproTC2 does not support SDRAM interface.

The FBC (frame buffer control) function can be bypassed by setting the bit 1 in the MISCTR0 (Misc. ConTrol Register 0, 0AH) register. To this, the frame rate conversion (includes de-interlacing) circuit will be disabled and the scaling function is performed upon the same frame rate as the input video.

Note that the registers 0xEA to 0xED are for SD/SGRAM mode setting, and registers 0xE6-0xE9 are for SD/SGRAM interface setting. Besides, a frame buffer test pattern can be defined and tested by the settings in FBC_PAT register (E5H) and the bit 7 (FILL_PAT) of FBCTR0 (E0H).

4.7.1 Initialization of FBC (Frame Buffer Controller) and SDRAM

1. Turn on the MCLK by setting the register FBC_BYPASS (FBCTR2[6]) to “0”and enable FBC block by set BYPASS register (MISCTR0 [1]) to “0”.
2. Program the SD/SGRAM mode setting registers (0xEA to 0xED) to proper value.
3. Toggle the register LMR_REQ(FBCTR0[6]) to load the SD/SGRAM mode data to SD/SGRAM. This will finish the initialization procedure of SD/SGRAM.

4.7.2 Self-test programming sequence of FBC

We provide a procedure which be used for testing the correctness of SDRAM access. The procedure is described as below:

Step1: Initialize the FBC as describe in 4.7.1 .

Step2: Set the FBC_BASE_ADDR to the starting address for testing access.

Step3: Set FBC_TEST_CN to “01”. This will set FBC_TEST_ACT to “1” and entering the Self-Test Mode of FBC.

Step5: Set FBC_TEST_CN to “81” then “01”. This will toggle FBC_VS and reset the FBC block.

Step6: Set FBC_TEST_CN to “41”, i.e. Set FBC_VACT to “1”.

Step7: Set FBC_TEST_CN to “61” then “41” "twice". This will toggle FBC_HS twice to start the SDRAM write access.

Step8: Set FBC_TEST_CN to “51”. This will FBC_HACT to “1”.

Step9: Generate a loop of I2C write access to FBC_TEST_PAT (xE4) with proper test pattern for 64 times.

Step10: Set FBC_TEST_CN to “01”.

Step11: Set FBC_TEST_CN to “21” the “01”. This will toggle FBC_HS to finish SDRAM write access.

Step12: Set FBC_TEST_CN to “09” then “01”. This will toggle FBC_SDRAM_RD to read 64 bytes of data from SDRAM to internal FIFO.

Step13: Read I2C register FBC_TEST_RESULT (0xEF) for 64 times. This will read back the internal FIFO data.

Step14: Compare the result data with the test patterns which you had written.

Step15: Set bit 0 of FBC_TEST_CN to “0” to exiting the Self-Test Mode

If the results are mismatched:

Solution1: Don't exit the Self-Test mode and repeat the procedure.

Solution2: Adjust the setting of register FBCTR3 (MCLK input/output delay) then repeat the procedure.

Note: "Toggle" means the operation of set and reset the corresponding bit.

4.7.3 Freeze and Vertical flip of the frame

When you set Freeze_FB(FBCTR2[7]) to “1”, you will enter the freeze mode and the frame is stilled.

When you set V_flip(FBCTR1[7]) to “1”, you can let the frame top/bottom reversal.

4.7.4 The DRAM supporting modes of ZiproSX

Input resolution	**Pixel rate (MHz)**	**Size and peak bandwidth needed**	**Output resolution**	**Configuration, data path, number of devices of SDRAMs, and offered bandwidth (overhead for access setup is supposed to be 15%)**		
				125MHz	100MHz	83MHz
1024*768 @75Hz	79	12 Mb, 287 MB/s	1024*768 @60Hz	1Mbx16, 16-bit path, x1 (212MB/s)		
800*600 @85 to 60Hz	56.25	7.32 Mb, 192.5 MB/s	800*600 @60Hz	1Mbx16, 16-bit path, x1 (212MB/s)	1Mbx16, 16-bit path, x1 (170MB/s)	
720*576i @60Hz	I13.5/ P27	12.66 Mb, 81 MB/s	720*576 @60Hz		1Mbx16, 16-bit path, x1 (170MB/s)	1Mbx16, 16-bit path, x1 (141MB/s)

NOTE:

1) Signal buffer is used for SVGA and XGA input.

2) Offered bandwidth is calculated by the formula: BW = Access speed*(data path/8)*(1-15%)

1024*768@75 to 60Hz: BW=(78.75+65)*16/8=287 MB/s, 1024*768*16/1024/1024=12 Mb
800*600@85 to 60Hz: BW=(56.25+40)*16/8=192.5 MB/s, 800*600*16/1024/1024=7.32 Mb
720*576I to P: BW=(13.5+27)*16/8=81 MB/s, 2*720*576*16/1024/1024=12.66 Mb

4.8 De-interlacing

t0947 chip converts the interlaced video signal into a progressive display. A motion-adaptive filtering refers to a mechanism using a decision on the presence and absence of motion. In the absence of motion, the best image can be obtained by simply merging even and odd fields which doubles the vertical resolution. However, in the presence of motion, this technique would suffer from motion artifacts. A de-interlacing circuit is used to interpolate the missing pixel using the intra-frame pixel data.

4.9 Gamma Correction RAM Tables

Gamma correction RAM tables are implemented after the Brightness/Contrast block to provide the color-mapping of the RGB data. The tables can be activated by setting GAMMAUSE (MSB of MISCTR0 or 0A hex) bit = 1. We can also by-pass the gamma correction function by resetting the GAMMAUSE bit = 0. Through three gamma table registers (GRWADDR, GGWADDR and GBWADDR) the data representing gamma curves can be put into the RAMs sequentially. These 10-bit gamma tables can be programmed by writing first the two MSB bits to high byte and the eight LSB bits to low byte for the first entity then the second and so on. And we can repeatedly program the register GRWADDR 512 times (high and low bytes for 256 entities). This will put the Red gamma curve into the Red RAM table (the first 10-bit data is written into RAM at address 0 and the 256th data is written into RAM at address 255). In a similar way, we can program the tables for Green and Blue channels.

4.10 CLUT, and Dithering

This chip embeds an On Screen Display function for human interfacing. It is designed to display colored patterns, icons or characters onto the screen. A 64 character fonts (downloadable from MCU) are provided for the application of Multi-language TV/Monitor. The Graphic Character Fonts can produce the effect of the pixel based graphic display, which allows the impressive display of the customized pattern or logos.

The OSD provides plentiful features to enhance the appearance of the displayed character fonts. Each character can have its own colors (up to 16 colors) and blinking option. Up to 10 shadowing modes (including bordering, boxing etc.) are provided together with 16 background colors. The versatile choice for display font color, background/shadow/window color, and shadow modes (including bordering and graphic character mode) leads to a unique OSD style. Some dynamic features, such as built-in see-through curtain effect, two-direction wipe in/out, character basis blinking, hardware overlapping windows etc. also enhance the image of OSD menu.

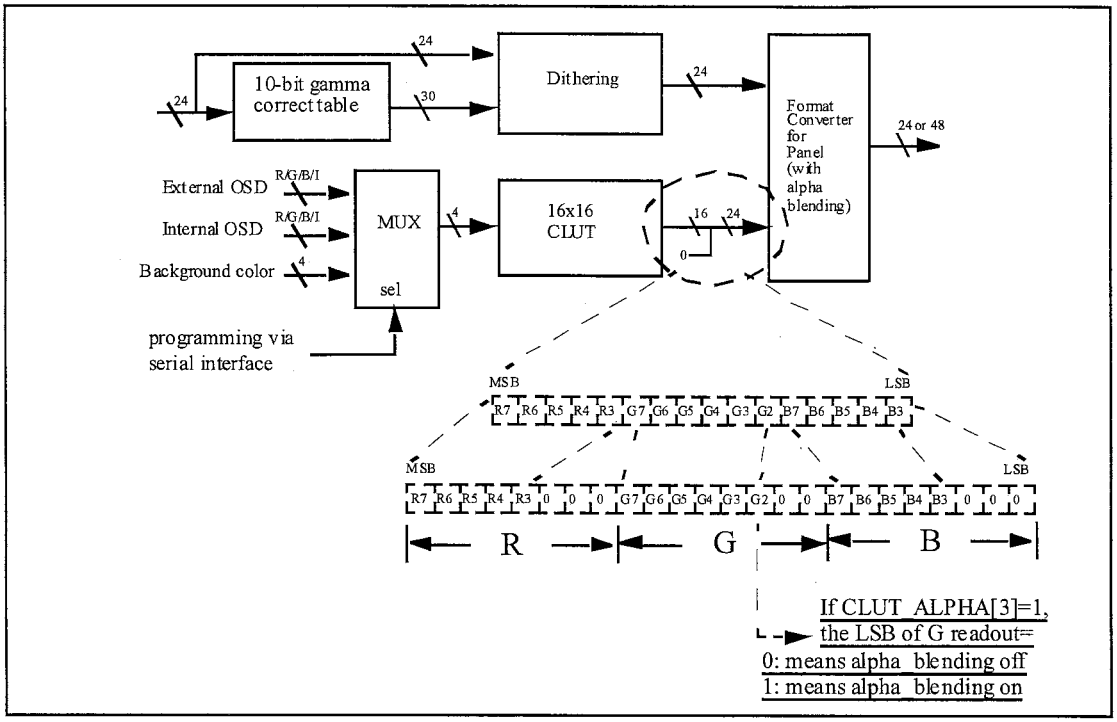
There is a 16x16 CLUT (color look-up table) which provides a programmable color palette for internal/external OSD and background color. The color index bus, namely R/G/B/I, is used as the address to the CLUT which defines the 16 colors for OSD and background color. The content and the index selection of CLUT are programming via serial interface. The mapping of the 16-bit RGB565 color to 24-bit true color is depicted as the following figure.

The format converter function for LCD panel also supports the dithering function. The related setting of dithering function are listed as below:

Function	Addr.(h)	Default Value	R/W	Description
DITHER_ON	x03[6:5]	00	W	00: no dithering (for the panel with 8 bit color depth per R/G/B) 01: 1 bit dithering (for the panel with 7 bit color depth per R/G/B) 10: 2 bit dithering (for the panel with 6 bit color depth per R/G/B) 11: 2 bit dithering (for the panel with 6 bit color depth per
DITHER_FDBK_ON	x05[1]	0	W	The error due to resolution change is fed back for dithering 0: feedback path is disconnected. 1: feedback path is connected for dithering.

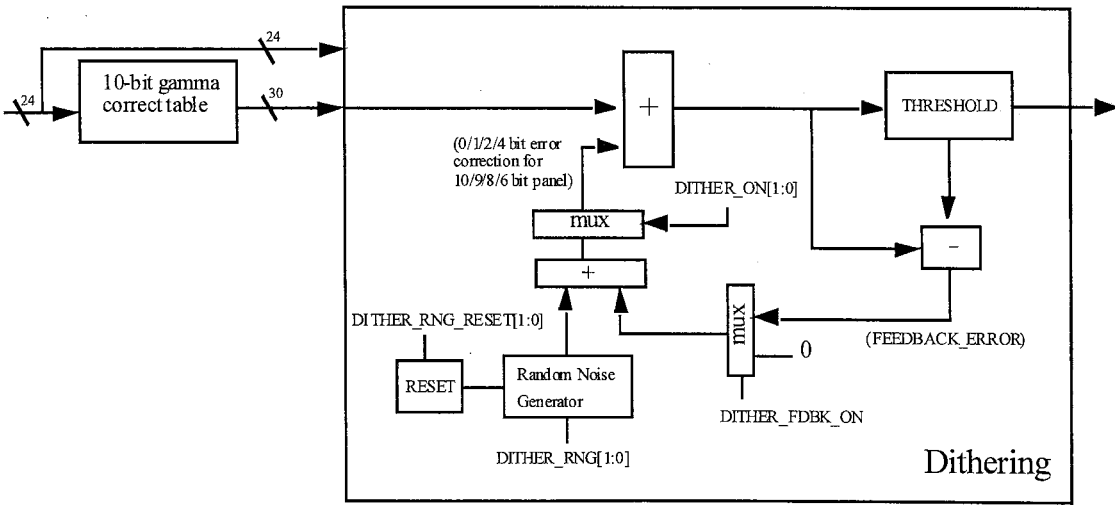
Function	Addr.(h)	Default Value	R/W	Description
DITHER_RNG	x0B[5:4]	00	W	DITHER RNG ON and choices. 00: RNG off 01: RNG 10 10: RNG 12 11: RNG 16
DITHER_RNG_RESET	x0F[4:3]	00	W	RNG reset selection when dithering is used. 00: No reset at all after system power-on reset. 01: RNG reset every VS. 10: RNG reset every 4 VS. 11: RNG reset every 16 VS. NOTE: Programming of RNG or FDBK_ON (feedback path is connected) can be found at OUTCTR2 and MISCTR1.
DITHER_TIME	x0F[1]	0	W	Dithering at spatial or time domain. 0: Dithering will be performed in spatial domain. Programming of RNG or FDBK_ON (feedback path is connected) can be found at OUTCTR2 and MISCTR1. 1: Dithering will be performed in time domain.
I_DITHER_ON	x1F[7:6]	00	W	00: no dithering operation for FBC input 01: Dithering at time domain. 10: 2 bit dithering at special domain for each R/G/B 11: 3 bit dithering at special domain for each R/G/B
I_DITHER_RNG	x1F[5:4]	00	W	Dithering operation for FBC input with RNG on and choices of cycling. 00: RNG off 01: RNG 10 10: RNG 12 11: RNG 16
I_DITHER_FDBK_ON	x1F[3]	0	W	The error due to resolution change is fed back for dithering operation to FBC input 0: feedback path is disconnected. 1: feedback path is connected for dithering.

FIGURE 11. Color look-up table for internal, external, and background color



4.11 Dithering and output formatter

The chip supports 8-bit or 6-bit panel using dithering methods as follows:



4.12 Power down

The chip enters into power down status by setting POWERDN pins to high. The system returns to normal after POWERDN is set to low.

In power down status, all circuits are set to off except the mode detection circuit which is always working.

4.13 Communication Protocol

The control of this chip can be achieved through two kinds of serial transfer, namely, SPI and 2-wire serial bus interface.

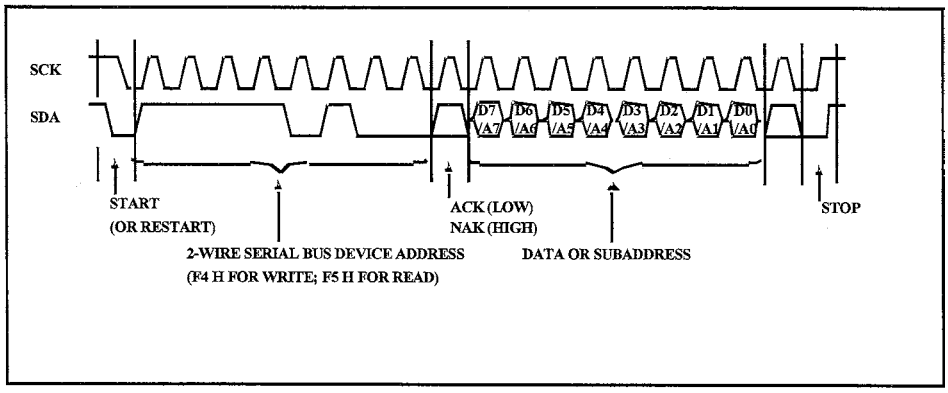
The selection between two kinds of interface can be done automatically by hardware. 2-wire serial bus interface also supports the read back of the some control registers.

The communication between this chip and MCU is performed by 2-wire serial bus interface or SPI interface. The industrial standard 2-wire serial bus interface supports bi-directional transfer (READ and WRITE) with baud rate up to 400 K bps. The 3-wire SPI interface can provide up to 1 M bps baud rate.

4.13.1 2-wire serial bus interface

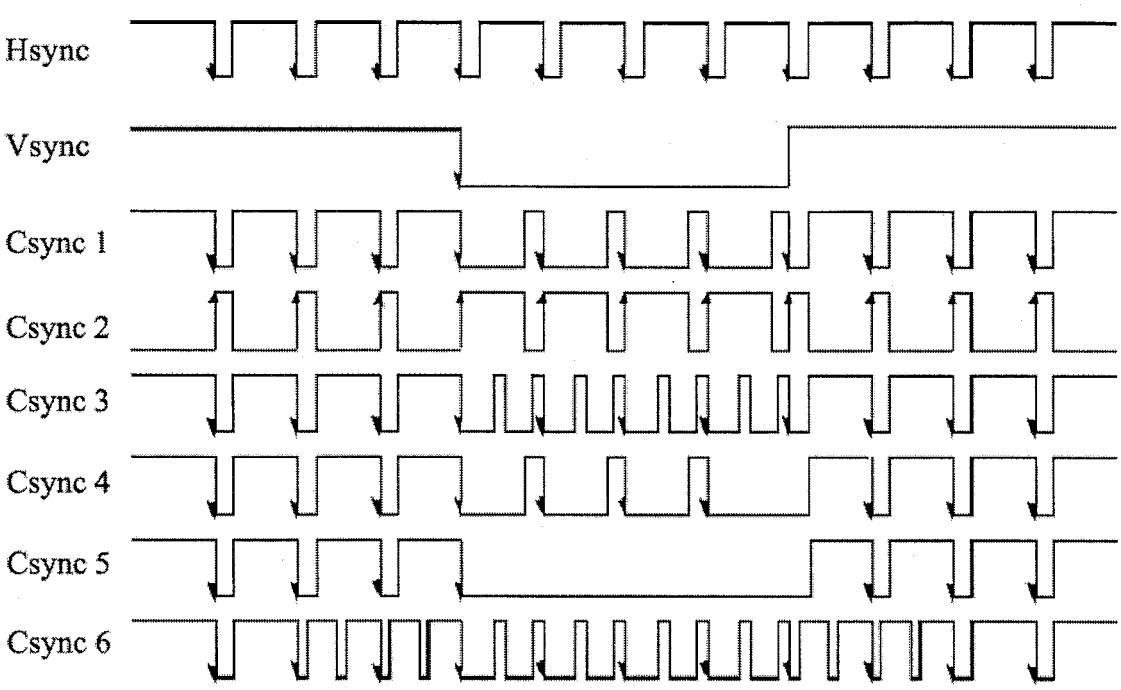
This chip supports the industrial standard 2-wire serial bus interface, which consists of SDA bi-directional data line and SCL clock line. The 2-wire serial bus slave address of this chip is 111000 (binary). The definition of the basic 2-wire serial bus interface protocol is illustrated as follows. For detailed timing and operation protocol, please refer to the standard 2-wire serial bus specification.

FIGURE12. The definition of the basic 2-wire serial bus timing protocol



4.14 Mode detection

The hardware mode detection circuit has the functions as mode detection blocks of all CRT monitor micro-controllers. For example, it can detect the presences, polarities, and frequencies of HS, VS, and DE. It sends out interrupt at certain programmable events, etc. Besides, there is a Vsync separation that handles six types of Csync inputs (depicted as in the following figure) and generate the corresponding Vsync pulse which can be used as the COAST signal into ADC chips. Generally, these Csync signals come from Hsync plus Vsync or Hsync exclusively OR Vsync or added serration pulse. The Composite sync to coast signal generation is depicted as in the following figure.



4.15 Auto-Adjustment

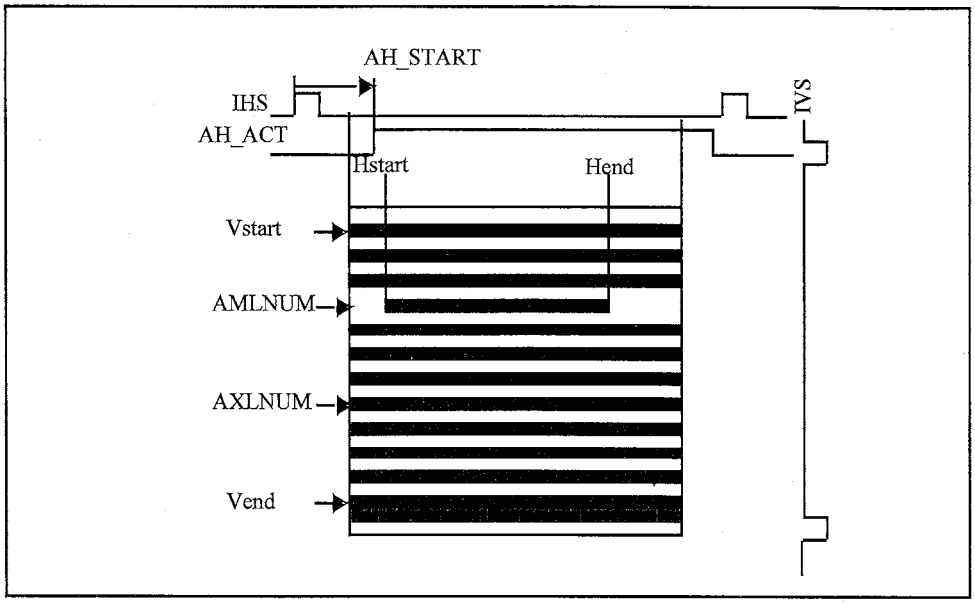
Searching a line for H-start, and H-end (if the Mth line designation is 00, the entire screen is searched)
A segment (including the full-line) of line is frozen and the RGB values can be read by host.
Optimum phase searching is via the calculation of the *sum of difference* of pixels in a window (including the entire screen) which is defined by IIC (for each RGB, or for the sum of RGB, for a frame, or for some frames) The *sum* of pixels on a window (including the entire screen) defined by IIC (for each RGB, or for the sum of RGB, for a frame, or for some frames) will be also performed.

While only *sum of difference* or *sum* operation (selected by IIC programming) is available for intra-frame operation, the *sum of difference* and *sum* operations are simultaneous available for inter-frame operations.

Besides, there are three functions supported by this chip, namely, line frozen, V start-end, and H start-end searching. The procedure are as follows:

1. Define a compare window: When the value of color channel R or G or B (designated by AACMP[1:0]) is greater than ARGB_MIN, a valid data is found. We use the parameter AH_START to define the starting location of searching window in horizontal direction. For vertical searching, the start point is the first line counted from the rising edge of IVS.
2. Check Vstart and Vend: When one line contain 2 (or greater than 2) valid data. The first valid line is named as Vstart and the last valid line is Vend.
3. Check Hstart and Hend: The parameter AMLNUM designates the line to perform the position searching of Hstart and Hend. Hstart is the first valid data and Hend is last valid data on the AMLNUM line. The RGB values of Hstart and Hend are also stored so that the value can be accessed by the host micro-controller.

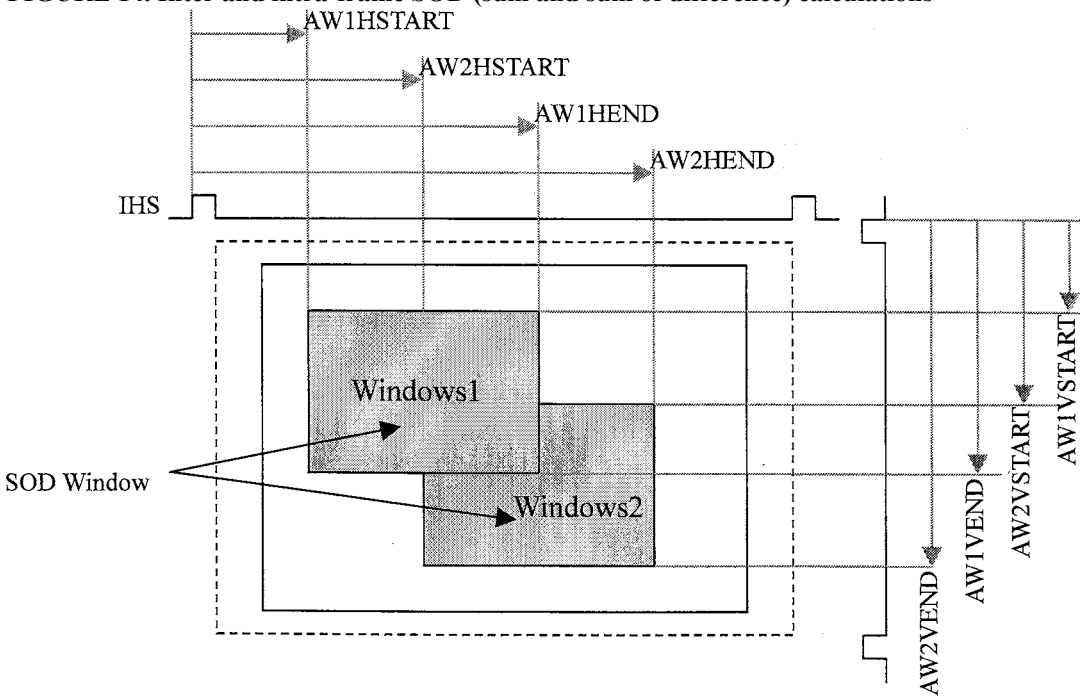
FIGURE 13. Parameters definition for auto adjustment.



4. To freeze a line buffer and read the content, one should designate the line address (counted from the first active line) and the starting pixel (counted from the H active region) and then read the same address AFZREAD sequentially.

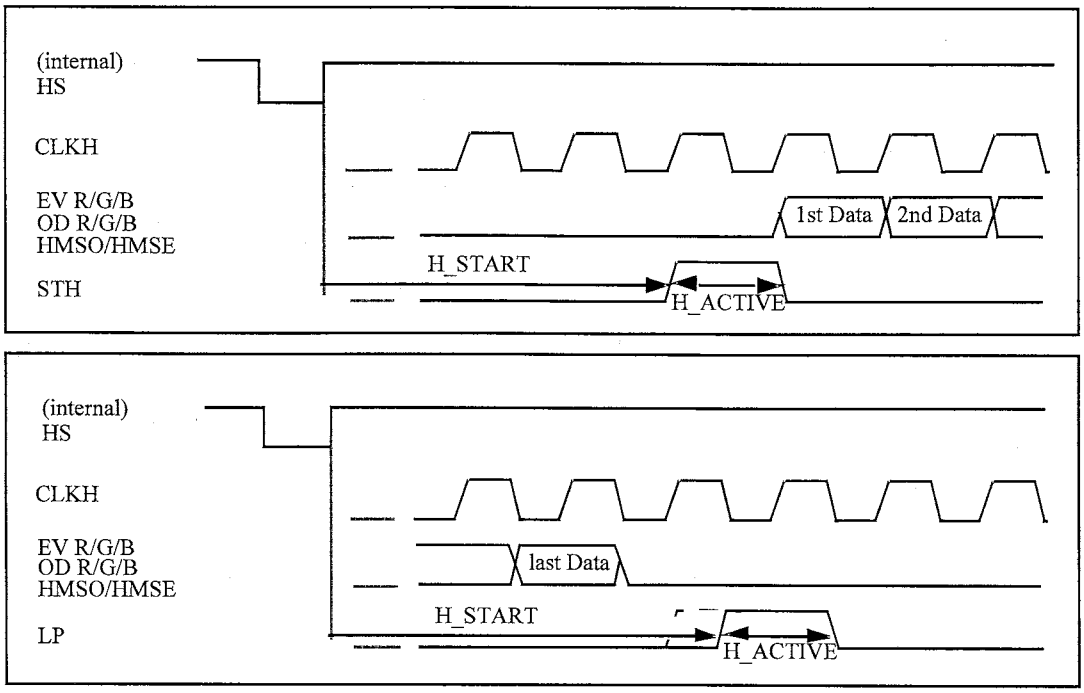
All data are updated per frame and check continuously.

FIGURE 14. Inter and intra-frame SOD (sum and sum of difference) calculations



4.16 Timing control

ZiproTC2 (t0949) chip includes a 2nd generation timing control circuit which drives the source and gate drives for 15" TFT-LCD panel. The output pins of this timing controller are shared with the SDRAM control pins. To this, the functions of timing control and SDRAM control are exclusive to each other. The timing control and SDRAM control circuits can both be deactivated.



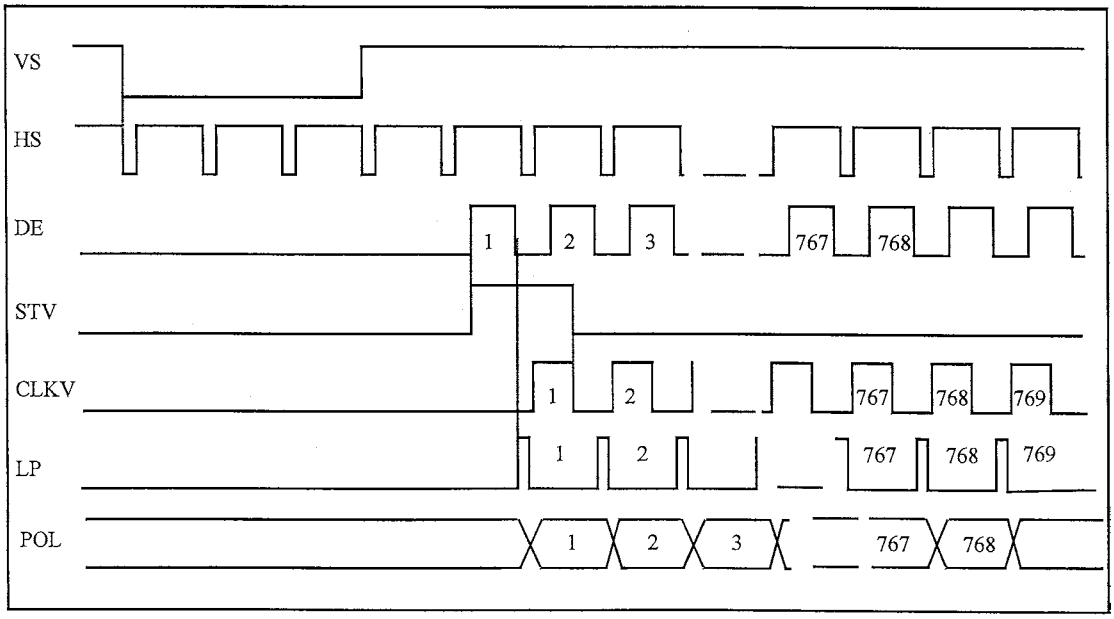


FIGURE 15. The generation of GPO0, GPO1, and GPO2 signals

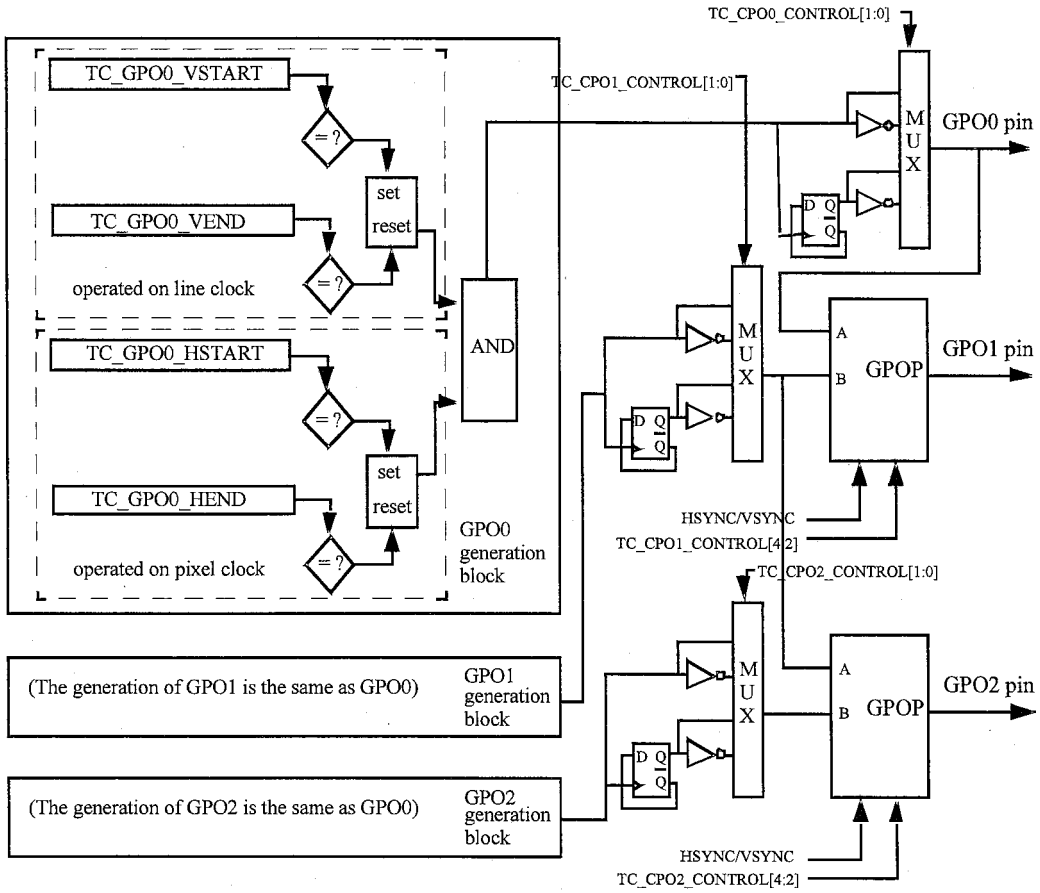
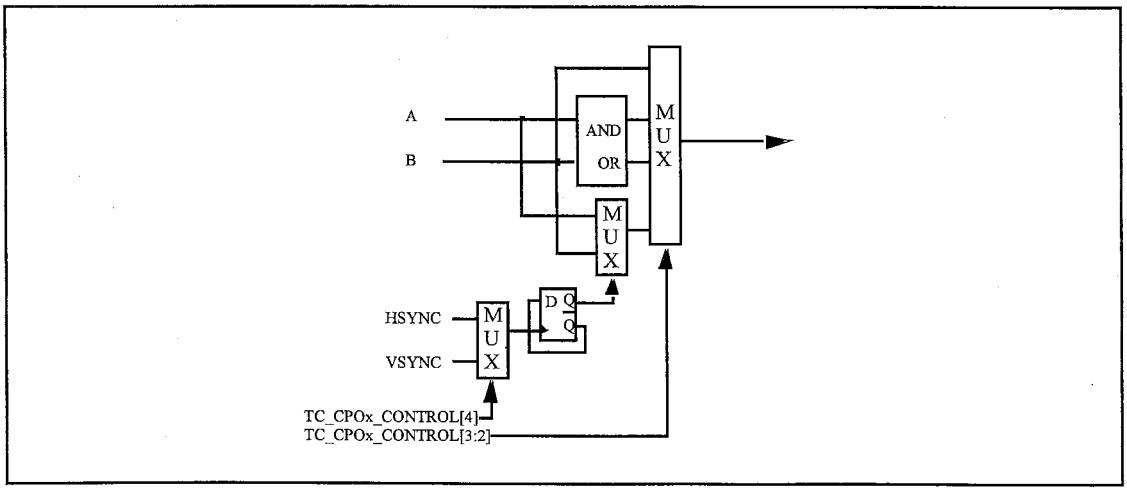
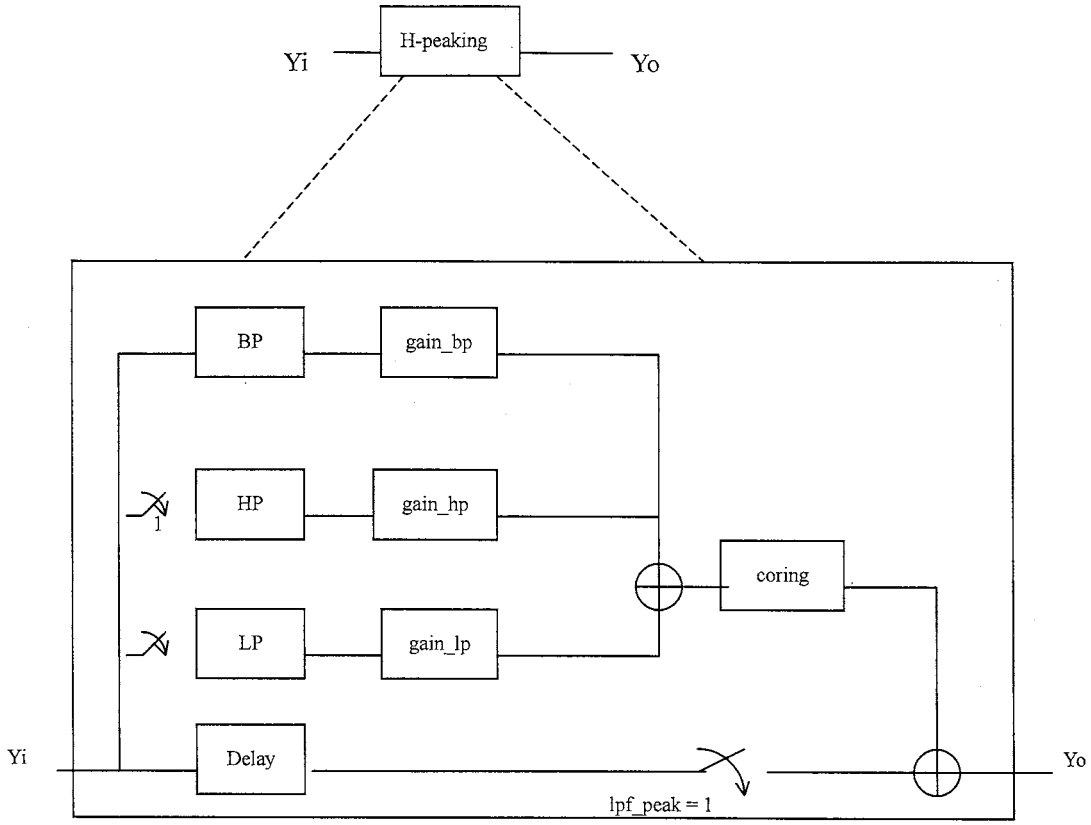


FIGURE16 .The GPOP (General Purpose OPeration) function



4.17 Peaking and noise-reduction

There are two main functions in the peaking block. One is implementing the PEAK function; the other is a programmable Low-Pass Filter (LPF). The object of PEAK function is to emphasis the high frequency part in order to increase the luminance sharpness. The programmable LPF can be used for noise-reduction.



In PEAK mode, $Yo = (\text{delay} + BP + HP)(Yi)$

In LPF mode, $Yo = (LP + BP)(Yi)$

where $BP = (1/8)*(1 - Z^{-2})^2$

$HP = (1/16)*(1 - Z^{-1})^4$

$LP = (1/16)*(1 + Z^{-1})^4$

Register for main control in peaking

35h bit 1	peaking enter	0 :enter	1 :bypass
35h bit 0	choose PEAK or LPF	0 :LPF	1 :PEAK

Register for PEAK

Peaking Control LSB (34h) bit [3:0]	gain_BP	**Peaking Control LSB** (34h) bit [7:4]	gain_HP
0000	0	0000	0
0001	0.25	0001	0.25
0010	0.5	0010	0.5
0011	0.75	0011	0.75
0100	1	0100	1
0101	1.25	0101	1.25
0110	1.5	0110	1.5
0111	1.75	0111	1.75
1000	2	1000	2
1001	2.25	1001	2.25
1010	2.5	1010	2.5
1011	2.75	1011	2.75
1100	3	1100	3
1101	3.5	1101	3.5
1110	4	1110	4
1111	5	1111	5

Register for LPF

Peaking Control LSB (34h) bit [3:0]	gain_LP
0000	0
0001	1/16
0010	2/16
0011	3/16
0100	4/16
0101	5/16
0110	6/16
0111	7/16
1000	8/16
1001	9/16
1010	10/16
1011	11/16
1100	12/16
1101	13/16
1110	14/16
1111	1

4.18 The Internal OSD

To program internal OSD, basically, two kinds of data, the data in Display RAM and data in the control registers must be filled via the serial transfer. The relationship between screen management and Display RAM is illustrated by a following figure, in the figure two OSD menu segments are stored in the Display RAM.

However, the menu stored from Row 4 to Row 8 are displayed. The content and characteristics of the displayed menu are defined by the data in the Display RAM. The starting row, which determine the selected menu segment, and the horizontal, vertical display positions are all programmed by the control registers.

4.18.1 The data structure in Display RAM

Basically, there are two kinds of data stored in the Display RAM:
1. the ROW attribute code: The ROW attribute for each row is always defined in the first column of each row. The row basis attributes are determined by the filled data, although the first column is invisible on the screen. The ROW attribute code consists of 16 bits, which are divided into 7 fields.
2.the displayed Character Font code: The data filled from Column 1 to Column 31 of each row (Row 0 to Row 15) are all treated as the Displayed Character Font code. So, the number of visible character locations will be 496 (16 X 31). The Character Font code consists of 2 fields. Font code field is represented by upper nibble (Bit 8 to Bit 15). The feature of each character font is decided by the lower nibble (Bit 0 to Bit 7), which forms the Character attribute field. However, the definition of the Character attribute field might vary with the different types of character font. There are three kinds of Character Fonts, Normal Character Font, Graphic Character Font and SPace font (code FF H is reserved as SP font code).

4.18.1.1 The ROW ATTRIBUTE

ROW Attribute															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Back I	Row Spacing				Programmable Character Height				CH	CW	Shadow mode				EOD

As shown in above table, there are 7 fields about the row based display attributes. Note the ROW attribute is always defined in the first column of each ROW (i.e. Display RAM location, 32XN, N = .15). The following sections will explain the details of each field.

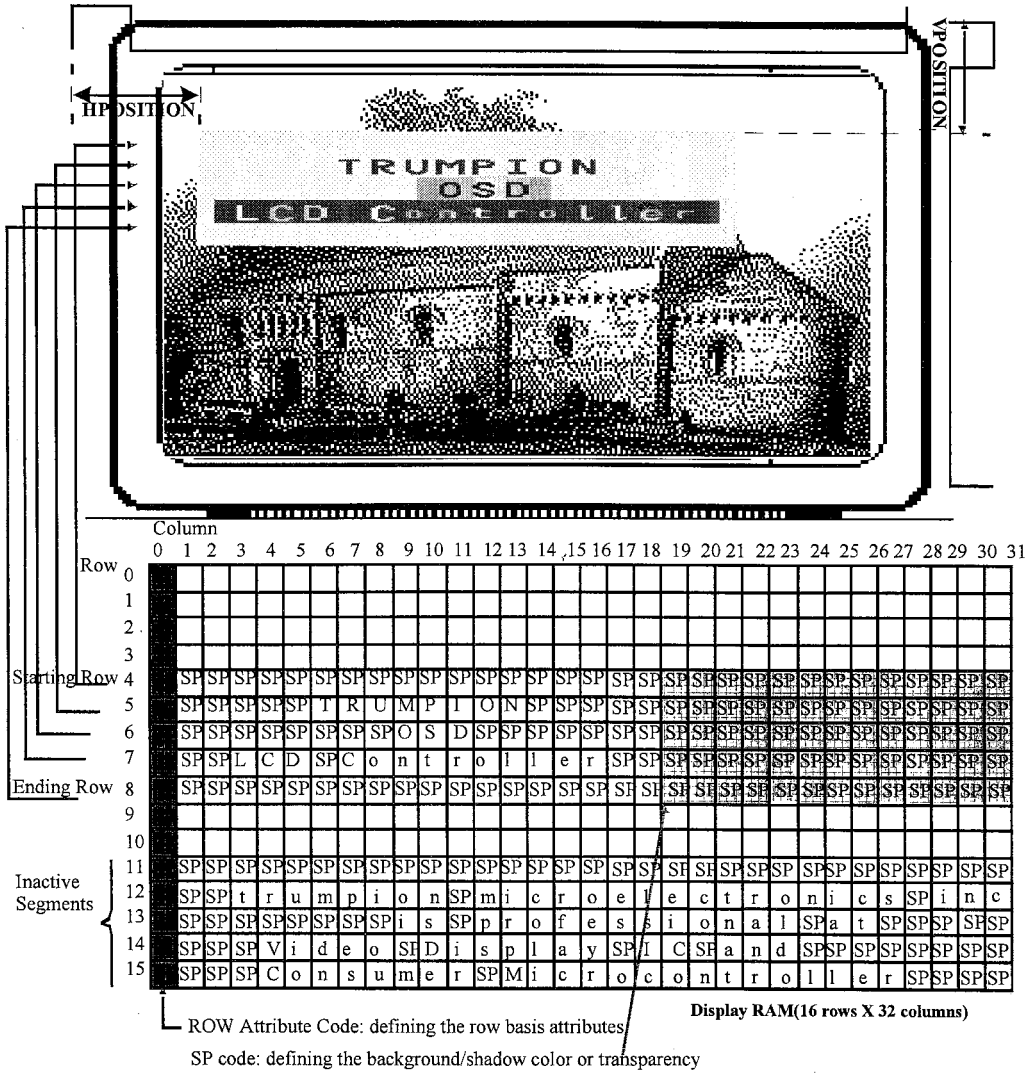


FIGURE17. The mapping between screen management and the Display RAM

4.18.1.1.1 The End of Display

ROW Attribute															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	**Bit0**
Back I	Row Spacing				Programmable Character Height				CH	CW	Shadow mode				**EOD**

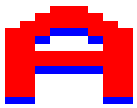
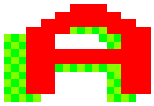
This field. ending of display (EOD), consists 1 bit, Bit 0. The bit value
0: stands for the continuation of the display data retrieved from the following rows in the Display RAM.
1: stands for the ending of data accessing from the next row in the Display RAM. The current row will be the final visible row on the screen.

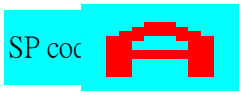
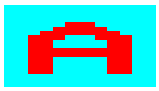
For the example shown upon, EOD bits of row 4, 5, 6 and 7 must be 0 and EOD bit for row 8 should be 1 to end the display.

4.18.1.1.2 The Shadow Mode

ROW Attribute															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	Bit0
Back I	Row Spacing				Programmable Character Height				CH	CW	**Shadow mode**				EOD

To enhance the appearance of the displayed character and accordingly highlight the self style of the end product, versatile shadowing modes are provided for each row. Thus, each displayed row can have different shadowing feature. *It is row basis feature*. This field is formed by 4 bits, Bit 1 to Bit 4. The shadow way associated with the corresponding code and example is illustrated in the following table.

SHADOW MODE	**REPRESENTATIVE CODE(B4 B3 B2 B1)$_B$**	**EXAMPLE PATTERN**
South shadow	(0000) $_b$	
West-South shadow	(0000) $_b$	
West shadow	(0010) $_b$	
West-North shadow	(0011) $_b$	
North shadow	(0100)$_b$	

East-North shadow	$(0101)_b$	
East shadow	$(0110)_b$	
East-South shadow	$(0111)_b$	
Bordering shadow	$(1000)_b$	
Boxing I	$(1001)_b$	
Normal	$(1010)_b$	
Boxing II	$(1011)_b$	SP code 

In principle, the shadow modes can be classified into four categories:

- Code 0000b to 0111b , and 1000b : The meaning of shadow is self-explained for this category except 1000b , bordering mode. It is assumed the sunlight coming from 8 directions, and accordingly generates shadow depending on the incident light. For bordering mode, the character font itself is surrounded by the shadow. Note the color of the shadow is word basis and decided by last SP code or SPdef control register (if no SP code is put in front of the concerned character)
- Code 1001b : This code stands for boxing mode. It is meant the character font is underlaid by the programmed background color. The background color is also defined by SP code or SPdef control register on the basis of word. Given by the flexibility of this mode, associated with SP code feature, it is already sufficient to create the window-like menu. In this mode, the background color defined by SP code takes effect from the left border of this SP code.

- Code 1010b : The normal character font without any shadow.
- □œ Code 1011b : This code stands for another type of boxing mode. It is similar to above boxing mode. However, the background color defined by SP code just takes effect from the right border of this SP code.

4.18.1.1.3 The Double width and /or Double Height

ROW Attribute															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	**Bit6**	**Bit5**	Bit4	Bit3	Bit2	Bit1	Bit0
Back I	Row Spacing				Programmable Character Height				**CH**	**CW**	Shadow mode				EOD

Two fields, CH and CW, are explained in this section. Despite of OSD dot rate synthesis for Character width, the line insertion for Character height, this is the most straightforward way to adjust the dimension of displayed menu by doubling the width or the height respectively.

The field. CW, consists of 1 bit, Bit 5. The bit value
0: stands for the normal character width, 12 OSD dots.
1: stands for the double size of character width, 24 OSD dots.

The field. CH, consists of 1 bit, Bit 6. The bit value
0: stands for the normal character height, (18 + inserted) scanning lines.
1: stands for the double size of character height, 2 X (18 + inserted) scanning lines.

FIGURE18. Four kinds of row dimension programmed by CH and CW

ROW Attribute

FIGURE18. Four kinds of row dimension programmed by CH and CW

4.18.1.1.4 The Programmable Character Height

ROW Attribute															
Bit15	Bit14	Bit13	Bit12	Bit11	**Bit10**	**Bit9**	**Bit8**	**Bit7**	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Back I	Row Spacing				**Programmable Character Height**				CH	CW	Shadow mode				EOD

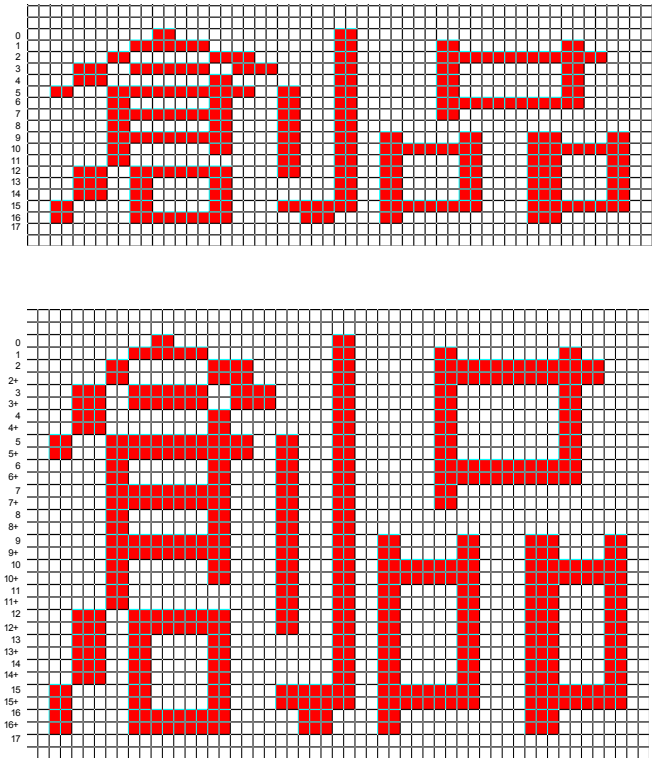
This field, Character Height Programming field, consists of 4 bits, Bit 7 to Bit 10. It provides more flexibility to adjust the vertical height of the displayed character/menu by BRM algorithm. Normally, the width of OSD can be well adjusted by varying the dot clock. However, the height of OSD can not be tuned as desired because it is limited to the number of scan line in the display system. The height of the character (accordingly, the height of OSD menu) is in inverse proportion to the number of the scan line per frame. To keep the compatibility, the height of OSD can be compensated by insertion of certain number of horizontal scan lines for each character in the same row.

In total, there are 15 possible line insertion encoded by this field. The following table illustrates the repeated lines for each corresponding code. This feature associated with CH bit and Row Spacing field (see next section) will provide variable character height from 5 scanning lines to 66 scanning lines.

Representative code (b10 b9 b8 b7) b	**Repeated line number: Normal Height(CH=0)/Double Height (CH=1)**	**Spacing No inserted lins CH=0 / CH=1**
0 0 0 0	None/None	0/0
0 0 0 1	9/19, 20	1/2
0 0 1 0	5, 13/11, 12, 27, 28	2/4
0 1 0 0	3, 7, 11, 15/7, 8, 15, 16, 23, 24, 31, 32	4/8
1 0 0 0	2, 4, 6, 8, 10, 12, 14, 16/5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25,26, 29, 30, 33, 34	8/16
0 0 1 1	5, 9, 13/11, 12,19, 20, 27, 28	3/6
0 1 0 1	3, 7, 9, 11, 15/7, 8, 15, 16, 19, 20, 23, 24, 31, 32	5/10
0 1 1 0	3, 5, 7, 11, 13, 15/7, 8, 11, 12, 15, 16, 23, 24, 27, 28, 31, 32 6/12	
0 1 1 1	3, 5, 7, 9, 11, 13, 15/7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28,31, 32	7/14
1 0 0 1	2, 4, 6, 8, 9, 10, 12, 14, 16/5, 6, 9, 10, 13, 14, 17, 18, 19, 20,21, 22, 25, 26, 29, 30, 33, 34	9/18
1 0 1 0	2, 4, 5, 6, 8, 10, 12, 13, 14, 16/5, 6, 9, 10, 11, 12, 13, 14, 17,18, 21, 22, 25, 26, 27, 28, 29, 30, 33, 34	10/20
1 0 1 1	2, 4, 5, 6, 8, 9, 10, 12, 13, 14, 16/5, 6, 9, 10, 11, 12, 13, 14, 17,18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 33, 34	11/22

Representative code (b10 b9 b8 b7) b	**Repeated line number:Normal Height(CH=0)/Double Height (CH=1)**	**No. of inserted lines CH=0 / CH=1**
1 1 0 0	2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16/5, 6, 7, 8, 9, 10, 13, 14, 15, 16, 17, 18, 21, 22, 23, 24, 25, 26, 29, 30, 31, 32, 33, 34	12/24
1 1 0 1	2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16/5, 6, 7, 8, 9, 10, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 30, 31, 32, 33, 34	13/26
1 1 1 0	2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16/5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	14/28
1 1 1 1	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16/5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34	15/30

One example which shows the effect of the line interpolation is demonstrated in figure19



This pattern is an example of character combination; It is formed by 5 characters combined in the horizontal direction.

B10 B9 B8 B7
1 1 1 1

Based on this configuration 15 lines are inserted in the vertical direction.

FIGURE19. The example of line insertion

4.18.1.1.5 The Row Spacing
4.18.1.1.5 The Row Spacing

ROW Attribute

ROW Attribute															
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Back I	**Row Spacing**				Programmable Character Height				CH	CW	Shadow mode				EOD

This field. Row Spacing, consists 4 bits, Bit 11, Bit12, Bit13 and Bit 14. The 16 possible row spacing are shown in the following table.

The first four codes are mainly for scaling down. The current displayed row can be reduced to 1/4, ½ and 3/4 of the original height. Following figure implies two possible applications for this feature. In the middle pattern, it is showing one spacing row with 5 scanning lines (thus, (Bit14, Bit13, Bit12, Bit11) = (0, 0, 1, 1)) are inserted between Row N and Row N+2. The right most pattern demonstrates the underline, at Row N+1, is added below the normal character font, A, located at Row N.

The remaining codes represent the lines inserted between two display rows. This feature can be used to adjust the vertical height, aspect ratio and accordingly avoid expansion distortion. The window, fade in/out feature remain valid for row spacing.

Representative code (b10 b9 b8 b7) b	**Repeated line number: Normal Height(CH=0)/Double Height (CH=1)**	**Spacing No. CH=0 / CH=1**
0 0 0 0	0 - 17 / 0 - 35 (No reduction)	18/36
0 0 0 1	0 - 4 / 0 - 9 (Upper 3/4 part displayed)	13/26
0 0 1 0	0 - 8 / 0 - 17 (Upper 1/2 part displayed)	9/18
0 0 1 1	0 - 12 / 0 - 25 (Upper 1/4 part displayed)	5/10
0 1 0 0	4 lines inserted between two rows	4
0 1 0 1	5 lines inserted between two rows	5
0 1 1 0	6 lines inserted between two rows	6
0 1 1 1	7 lines inserted between two rows	7
1 0 0 0	8 lines inserted between two rows	8
1 0 0 1	9 lines inserted between two rows	9
1 0 1 0	10 lines inserted between two rows	10
1 0 1 1	11 lines inserted between two rows	11
1 1 0 0	12 lines inserted between two rows	12
1 1 0 1	13 lines inserted between two rows	13
1 1 1 0	14 lines inserted between two rows	14
1 1 1 1	15 lines inserted between two rows	15

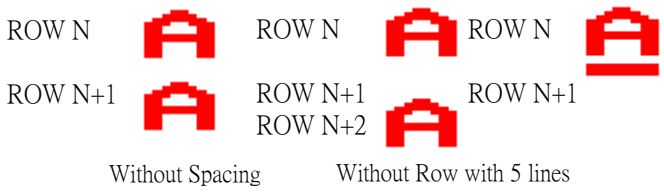


FIGURE 20. Spacing between two displayed rows and underline effect

4.18.1.1.6 The Row Spacing

ROW Attribute															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Back I	Row Spacing				Programmable Character Height				CH	CW	Shadow mode				EOD

This field, intensity bit for background color (Back I) for current row, consists 1 bit, Bit 15. The bit value

0: The background color defined by the character attribute (Bit7, Bit6, Bit5) is not intensified.

1: The background color defined by the character attribute (Bit7, Bit6, Bit5) is intensified.

Accordingly, in term of row basis, the background colors can be extended to 16 colors.

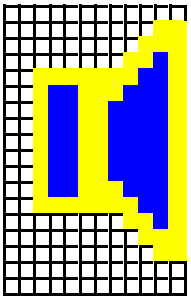
4.18.2 CHARACTER FONT CODE

Bit15 Bit14 Bit13 Bit12 Bit11 Bit10	Bit9 Bit8 Bit7	Bit6	Bit5	Bit4	Bit3 Bit2 Bit1 Bit0			
Font code attribute								
Ad7 Ad6 Ad5 Ad4 Ad3 Ad2	Ad1 Ad0 BR	BG	BB	R	G	B	I	Blink

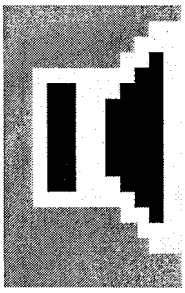
The Normal Character Font (NCF) and the Graphic Character Font (GCF) are both encoded by 8 bits (Font code field; Bit 8 to Bit 15). Each Character Font occupies 20 words to form one Character Font. In addition to 18 words (12 bits per word), 2 more words are added to keep the data of last row and look ahead the data of next row. Accordingly, even for the case of vertical combination of two characters, it is still possible to render the complete shadow and bordering modes.

The characteristics of the Normal Character Font (NCF) is specified by Font Code Attribute. Bit 7 to Bit 5, associated with the intensity bit determine the background color underneath the foreground dot. The foreground color of this character font is defined by the R, G, B, I bit, Bit 4 to Bit 1 from the Font Code Attribute. A character basis blinking is achieved by Bit 0, blink bit. There are two blinking rates programmed by Bit 2, CF, in the control register, OSDCTRL.

The character font with address greater than value, predefined by the register, Graphic_start, is treated as Graphic Character Font or Multi-Color Font. Accordingly, the font number of Graphic Character Font is not fixed and dependent of the customer need. Nevertheless, font code address, FFH (i.e. 11111111b) is reserved for the Space code. The Graphic Character Font will consume three times of words, since R, G, for each OSD dot will be defined in separate Character Font domain. Note the three consecutive font address will be bound to this Graphic Character Font. For the ROM coding scheme of the graphic character font. Regarding character attribute of the graphic font, bit 2 to bit 7 are meaningless. If Bit 1 is set, the undefined dot (i.e. 000b) is filled by background color, which is specified by last Space code. Bit 0, Blink, is still effective in the programmed blinking rate. The background color underneath the multi-color dot is stationary and not blinked. The following diagram illustrates Graphic Character Font in two modes, decided by the setting of Bit 1.



Graphic Character Font
with Bit 0 cleared



Graphic Character Font
with Bit 1 set

The background color, green,
is defined by last SPACE code

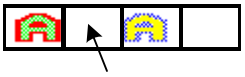
FIGURE 21. Two types of the Graphic Character Font; GCF with Background color and GCF without Background color

4.18.3 THE SPACE CODE

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved SP code (FF H)								Space code attribute							
1	1	1	1	1	1	1	1	-	-	-	R	G	B	I	SPT

The SPace code is in fact a special case of Character Font. One dedicated font code, FF H, is reserved as the Space code. Space code attribute (Bit 0 to Bit 4) defines the functioning of the SPace code. However, depending on the setting of Row Attribute, the functioning of SPace code could be different. Typically, there are following cases:

- If one of shadow codes, 0000b to 0111b , and 1000b , the SPace code is used to change the color of shadow. The shadow color is encoded by R, G, B and I bit. The domain of SPace code, itself is transparent. Therefore, Bit SPT is meaningless in this case. One example for this case is shown below.



Space code =>Change shadow color in bordering mode
from Red to Blue

FIGURE 22.SPace code is used to change the shadow color

- If the boxing mode, code 1001b, or code 1011b, is chosen from the shadow mode, then the SPace code is used to change the background color, which is defined by R, G, B and I bit. In this case, the background color is rendered immediately from the domain of the SPace code itself (in the case of 1001b) or rendered right after the domain of the SPace code (in the case of 1011b). However, if SPT bit is set, the background color will disappear and become transparent. If the color change is expected in the midway instead of the starting of SPcode domain, then, one bit, Split, in OSDCTRL register must be set illustrates the situation mentioned for this case.

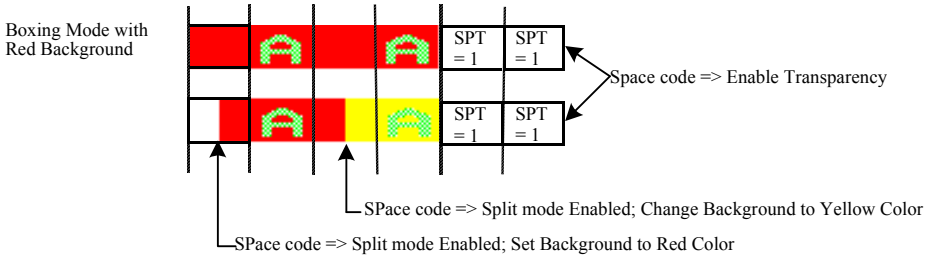


FIGURE 23. SPace code is used to change the background color in boxing mode and used for

- If the code, 1010b , (i.e. the normal mode) is selected, SPcode is meaningless in this case.

4.18.4 Font ROM and RAM Code Generation

The ZiproSX OSD contains a font ROM and a font RAM. The ROM contains 192 fixed character code and the RAM provides 64 character space for downloadable fonts for the customer's special requirement. The character and graphic font (multi-color font) can both download to the font RAM. To satisfy different application needs, the number of the character and graphic character fonts can be customized. The normal character font and the graphic character font share the same character RAM. However, note the RAM space required by the graphic character font is three times of the normal character font. In other words, every graphic character font will occupy the space of three normal character fonts. The trade-off is determined by the application. The location range of the graphic character font is defined by registers Graphic_start (3EH) and Graphic_end (3FH) and each graphic font is formed with 3 consecutive font sites.

4.18.4.1 NORMAL CHARACTER FONT CODE

The visible character matrix is 12 columns by 18 rows. However, in order to keep the completeness o shadowing/bordering effect in the case of vertical combination, two additional rows are provided. It is illustrated by the following diagram. Normally, Row 0 and Row 19 are filled with 0. However, it is not necessary for users to take care of such subtle issues. A paint brush like font generator is provided to generate font code.

4.18.4.2 GRAPHIC CHARACTER FONT CODE

The graphic character font can be placed from the address pointed by Graphic_start in the RAM space with three consecutive font sites. The paint brush like font generator can help the user to generate the graphic character font. The following figure demonstrates the graphic character font coding scheme, although it is transparent to the user.

Each dot in the graphic character font is encoded by three bits, which are corresponding to R, G, B colors. The color definition by 3 bits (R, G, B) is shown in the following table:

COLOR	BIT2 (R)	BIT1 (G)	BIT0 (B)
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Black	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Although the cyan color is not defined, there are two ways to render the cyan color. The window with cyan color underline the color font can make the dots with 000b become cyan dots. In fact, 16 colors can be applied to the window. So, it is also possible to render other colors for dot with 000b code. The second approach is enabling Bit 1, I, of character attribute. Then the dot of graphic character font with 000b can be filled by the background color, which is defined by last SPACE code. There are 16 colors for the background color, including cyan color.

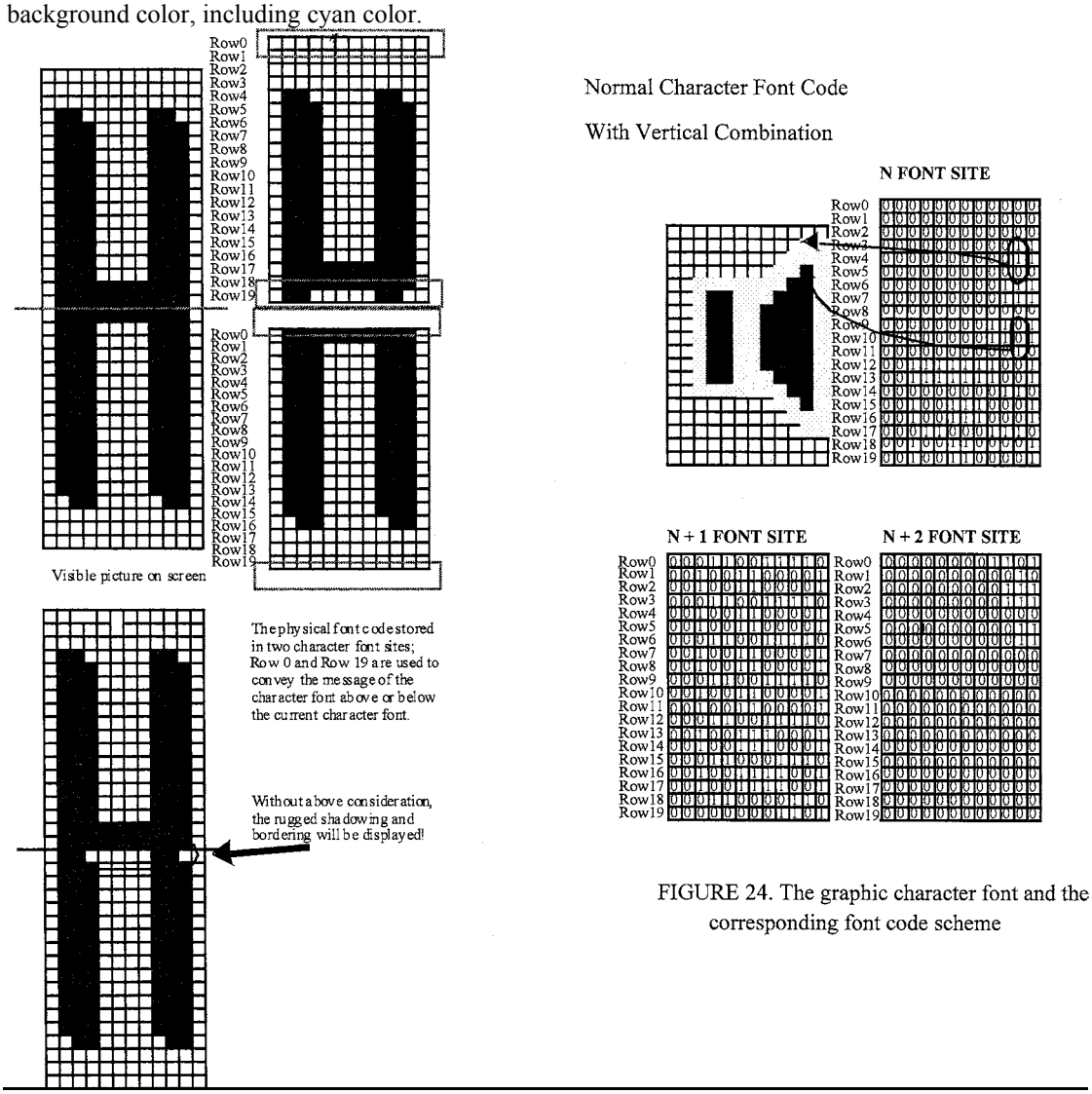


FIGURE 24. The graphic character font and the corresponding font code scheme

5.0 REGISTER DEFINITION

The 2-wire serial bus slave address of this chip is 1111000 (bin) (or F0 hex):

TABLE 20. PANORAMA OF SUB-ADDRESS REGISTER

	LOW NIBBLE OF SUBADDRESS																
HIGHNIBBLE	Addr(hex)	X0H	X1H	X2H	X3H	X4H	X5H	X6H	X7H	X8H	X9H	XAH	XBH	XCH	XDH	XEH	XFH
	0XH	ID_VER	IN_CTR		OUT_CTR			IN_CTR2	IN_CTR3	IN_CTR4	OUT_CTR3	MISCTR		STATUS0	STATUS1	INTCTR	MISCTR2
	1XH	INPUT WINDOW PARAMETERS													IVHREF_DELAY	IVS_DELAY	IN_CTR5
	2XH	AUTO ADJUST PARAMETERS															
	3XH					PEAKING		OUTPUT WINDOW PARAMETERS									
	4XH	BACKGROUND WINDOW PARAMETERS								DE DIM WINDOW PARAMETERS							
	5XH	PANEL BACKGROUND PARAMETERS						OSD PARAMETERS							PWM		
	6XH	SCALING PARAMETERS															
	7XH	SCALING PARAMETERS				AUTO ADJUST PARAMETERS					PWM	MISC (CLAMP)		IHV_DELAY4WRAP			
	8XH	AUTO ADJUST PARAMETERS															
	9XH	AUTO ADJUST PARAMETERS								AUTO ADJUST PARAMETERS						LB_MARGIN	
	AXH	ICLK/PCLK MEASURE PARAMETERS (It was for AUTO ADJUST)									PX_AS_ALINE	AUTO ADJUST PARAMETERS				BRIGHTNESS, CONTRAST	
	BXH	BRIGHTNESS, CONTRAST, GAMMA, CLUT, and ALPHA BLENDING										PLL PARAMETERS					16:9
	CXH	DEno_perV		OSD freq		IN/OUT HS/VS PARAMETERS						OSD PARAMETERS					
	DXH	HARDWARE MODE DETECTOR PARAMETERS											KEYSTONE PARAMETERS				
	EXH	Frame buffer control and related															
	FXH	JPEG WRITE, 16:9 ZOOMING, DEINTERLACE, and PWMR0/B0															

TABLE 21. I/O CONTROL REGISTER

REGISTER FUNCTION	Addr (hex)	D7	D6	D5	D4	D3	D2	D1	D0
Chip ID and Version (ID_VER)	00H								
Input Control Register0 (INCTR0)	01H (R/W)	DIS_IHSPOL	IHS_POL	IRGB24AB	DEINTERLACE_ON	DE_ONLY	DE_DELAY(2)	DE_DELAY(1)	DE_DELAY(0)
Input Control Register1 (INCTR1)	02H (R/W)	ICLK_INV	ODD_POL	INCODE	YUVF	IRGB48(1)	LBRV	IRGB24	IRGBEN
Output Control Register0 (OUTCTR0)	03H (R/W)	RELD_FHADR	DITHER_ON(1)	DITHER_ON(0)	PCLK_INV/PHCLK_INV	PCLK_OP (2)	PCLK_OP (1)	PCLK_OP (0)	PRGB48
Output Control Register 1 (OUTCTR1)	04H (R/W)	PVS_POL	PHS_POL	POUT_OFF	BKFRC	BKCOL(3)	BKCOL (2)	BKCOL (1)	BKCOL (0)
Output Control Register 2 (OUTCTR2)	05H (R/W)	DEINTERLACE_AUTO [1]	DEINTERLACE_AUT O [0]	HUE_SAT_ADJUST	PCLKIN_EXT	OVS_VACTIVE	PDE_POL	DITHER_FDBK_ON	PABCLK_EN
Input Control Register2 (INCTR2)	06H (R/W)	IYUV444_PEG [1]	IYUV444-JPEG [0]	XTAL_PULSE_SEL[1]	XTAL_PULSE_SEL[0]	IVS_SELE CT	IVS2PVS	IVS_DIV_2	FIELD_DETECT_IN
Input Control Register3 (INCTR3)	07H (R/W)	USE_IHRE F	USE_IVRE F	IH_INV4FID	IV_INV4FID	ICLK_DELAY[2]	ICLK_DELAY[1]	ICLK_DELAY[0]	FID_INV_SCALER
Input Control Register4 (INCTR4)	08H (R/W)	IA_A2PORT	IB_B2POR T	ICLKDIV2_EN	IHVSA_B	IBCLK_DELAY[2]	IBCLK_DELAY[1]	IBCLK_DELAY[0]	FORCE_UP_DN
Output Control Register3 (OUTCTR3)	09H (R/W)	FID32_CLAMP[1]	FID32_CLAMP[1]	PCLKEQICLK	NTSC_HDTV	RST_GT_ADR	H_FLIP	PWMR0ACT	PWMB0ACT
Misc. Control Register 0(MISCTR0)	0AH (R/W)	GAMMAUSE	DEINT_OFIF_32PD	VHSYN_SEL	FREEZE	EOSD_EN	EOSDFR	BYPASS	DE_DIM_EN

REGISTER FUNCTION	Addr (hex)	D7	D6	D5	D4	D3	D2	D1	D0
Misc. Control Register 1(MISCTR1)	0BH (R/W)	MATRIX_ ON	INVMATRI X_ON	DITHER_R NG(1)	DITH ER_RNG(0)	EOSD_SY NSEL	CLAMP_O FF	BACLK_S EL ADCLKEN	IIC_ACT_ DIRECT
Status Register (STATUS0)	0CH (R)								
Status Register (STATUS1)	0DH (R)	CINEMA	MOTION_ VIDEO				ASOD_RD Y		AML_RDY
Interrupt Control Register (INTCTR)	0EH (W)	INTEN							
Misc. Control Register2 (MISCTR2)	0FH (R/W)	OVCLK_D ELAY[2]	OVCLK_D ELAY[1]	OVCLK_D ELAY[0]	DITHER_R NG_RESET (1)	DITHER_R NG_RESET (0)	VIDEO_F REERUN	DITHER_T IME	RGB12_DE _DELAY
Input Control Register5 (INCTR5)	1FH (R/W)	I_DITHER_ ON (1)	I_DITHER_ ON (0)	I_DITHER_ RNG (1)	I_DITHER_ RNG (0)	I_DITHER_ FDBK_ON	HMD_VF_ CNT1	HMD_VF_ CNT0	HS_EQ_HR EF
SOD Control Register (SODCTR)	77H (R/W)	SOD_FRAM E_NO[3:0]							SOD_INTR A
SOD Mask Register (SODMASK)	78H (R/W)	SOD_MAS K_BIT[2:0]					SOD_R_M ASK	SOD_G_M ASK	SOD_B_MA SK
OSD control register0 (OSDCTR0)	CEH (R/W)	VITOREND L	VINT	TEST0	ETF	R	G	B	I
OSD control register1 (OSDCTR1)	CFH (R/W)	SPLIT	HTONE	MONITOR	HP	VP	BP	BF	IODS_EN

ID_VER (Chip ID and Version, 00H)			Default
7-0	ID_VER	01000001 (bin, for t0944/t0946/t0947/t0949)	41
7-0	ID_VER	01010001 (bin, for ZiproSO/t0959)	51

INCTRO (Input ConTrol Register 0, 01H)			Default
7	DIS_IHSPOL	0: Auto detecting function of the polarity of HS of input video will be checked automatically 1: Auto detecting function of the polarity of HS of input video will be disabled Note: The polarity of VS of input video will be checked automatically	0
6	IHS_POL	0: The rising edge of input HS will be used as the start of the sync pulse 1: The falling edge of input HS will be used as the start of the sync pulse	0
5	IRGB24AB	0: Input RGB 24-bit data use A port 1: Input RGB 24-bit data use B port	0
4	DEINTERLACE_ON	0: Deinterlace function off 1: Deinterlace function on Note: Panel Vertical Active EVEN Start, Panel Vertical Active ODD Start, Panel Vertical EVEN Total, and Panel Vertical ODD Total should be defined before Deinterlace function set to on	0
3	DE_ON	0: The H and V sync signals are used for synchronizing the display data. 1: The DE (Display Enable) signal is used for synchronizing the display data.	0
2-0	DE_DELAY [2:0]	DE signal can be delayed or advanced for the matching of display data vs enable signal. This signal is valid only if DE_ON=1. 0xx: No delay (x means do not care) 100: -2 clock delay. 101: -1 clock delay. 110: +1 clock delay. 111: +2 clock delay.	000

INCTR1 (Input ConTrol Register 1, 02H) Default			Default
7	INCLK_INV	INCLK invert enable 0: normal input clock 1: invert input clock	0
6	ODD_POL	ODD indicate polarity (inside use only) 0: 1st field is ODD and ODD is ACTIVE HIGH 1: 1st field is ODD and ODD is ACTIVE LOW	0
5	INCODE	0: input video code is binary offset 1: input video code is 2 complement	0
4	YUVF	0: 16 bit YUV422 1: 8 bit YUV422 (CCIR 656)	0
3		reserved	0
2	LBRV	Line Buffer Reset Value Select 0 : the line buffers are reset to x000000 1 : the line buffers are reset to x008080	0
1	IRGB24	1: RGB 24 bits input Note: t0947/0949 can accept 24-bit or 12-bit input. But IRGB24 should be set to 1 always.	1
0	IRGBEN	0: YUV input 1: RGB input	1
INCTR2 (INput ConTrol Register 2) has the sub-adress at 06H.			

OUTCTR0 (Output ConTrol Register 0, 03H) (This register can be read and write)			Default
7	RELD_FHADR	Reload Freeze Address The starting address of frozen line which will be reloaded if a low to high transient detected. Please refer to the register 84 and 85 for more detail.	0
6:5	DITHER_ON (1:0)	00: no dithering (for the panel with 8 bit color depth per R/G/B) 01: 1 bit dithering (for the panel with 7 bit color depth per R/G/B) 10: 2 bit dithering (for the panel with 6 bit color depth per R/G/B) 11: 2 bit dithering (for the panel with 6 bit color depth per R/G/B)	00
4	PHCLK_INV	0: Normal PHCLK clock output to panel 1: Inverted PHCLK clock output to panel (The relationship of PHCLK and PCLK is also defined by PHCLK_OP(1:0) and PRGB48)	1

3:1	PHCLK_OP (2:0)	Phase deviation of PHCLK with respect to PCLK 000: No delay 001: Delay 1 unit 010: Delay 2 units 011: Delay 3 units 100: Delay 4 units 101: Delay 5 units 110: Delay 6 units 111: Delay 7 units (The relationship of PHCLK and PCLK is also defined by PHCLK_INV and PRGB48).	000
0	PRGB48	0: Single pixel output per panel clock (the frequency of PHCLK is equal to PCLK, the phase is defined by PHCLK_INV and PHCLK_OP(1:0)) 1: Double pixel output per panel clock (the frequency of PHCLK is equal to half of PCLK, the phase is defined by PHCLK_INV and PHCLK_OP(1:0))	1

OUTCTR1 (OUTput ConTrol Register 1, 04H)			**Default**
7	PVS_POL	PVS output polarity (inside use active High) 0: Negative polarity (active Low) 1: Positive polarity (active High)	0
6	PHS_POL	PHS output polarity (inside use active High) 0: Negative polarity (active Low) 1: Positive polarity (active High)	0
5	POUT_OFF	Panel output control & data disable 0: PHS, PVS,DEN,PRED/GRN/BLU, and P2RED/GRN/BLU output are enabled. (or PARED/GRN/BLU or PBRED/GRN/BLU in ZiproSO) 1: PHS, PVS,DEN,PRED/GRN/BLU, and P2RED/GRN/BLU output are set to weak pull low.(or PARED/GRN/BLU or PBRED/GRN/BLU in ZiproSO)	1
4	BKFRC	Panel output Force to Background color 0: Normal Panel output 1: Output Panel is forced to Background color, the color is selected by BKCOL[3:0]	0
3:0	BKCOL[3:0]	Panel output Background color select signals. These signals share the look-up table with OSD to generate colors.	000

OUTCTR2 (OUTput ConTrol register 2, 05H)			Default
7-6	DEINTERLACE_AUTO [1:0]	The way deinterlacing circuit will work. 00: Deinterlacing circuit is always off. 01: Deinterlacing circuit is always on. 1x: reserved	00
5	Reserved		0
4	PCLKIN_EXT	The way PCLK, panel clock, is generated. 0: PCLK is generated by internal PLL. 1: PCLK is fed from PCLKIN pin (by external source).	0
3	OVS_VACTIVE	The OSD VS output is generated using 0: Overlay VS as in Zurac1. 1: Vertical display active signal.	0
2	PDE_POL	0: active High for display data enable output to panel 1: active Low for display data enable output to panel	0
1	DITHER_FDBK_ON	The error due to resolution change is fed back for dithering 0: feedback path is disconnected. 1: feedback path is connected for dithering.	0
0	Reserved		

INCTR2 (Input ConTrol Register 2, 06H)			Default
7-6	IYUV444_JPEG[1:0]	Additional input modes. The default mode is 00 for Zurac2 compatible. 00: RGB input or 8-bit YUV422 or 16-bit YUV422 input modes as defined by INCTR1 (02hex) 01: input is YUV444. 10: JPEG write modes or segment write via 8-bit YUV422 and HREF input pins 11: RGB12. NOTE: RGB12 bus uses the IRED[7:0] and IGRN[7:4] pins. The bus will be expanded to 24 bits RGB internally.	00
5-4	XTAL_PULSE_SEL[1:0]	Crystal clock pulse selection. This clock pulse will then be counted by ICLK and PCLK. 00: 1024 crystal clocks. 01: 2048 crystal clocks. 10: 3072 crystal clocks. 11: 4096 crystal clocks.	00
3	IVS_SELECT	Input VS source selection. 0: from external IVS, 1: from internal mode detection circuit.	0

2	IVS2PVS	PVS generation using the rising/falling edge of IVS (For the case PVS is generated by free-running, this control bit is invalid) 0: falling edge. 1: rising edge.	0
1	IVS_DIV_2	Input VS frequency will be divided by 1 (no changed) or 2. 0: normal, 1: input VS frequency will be divided by 2	0
0	FIELD_DETE CT_OFF	0: Field detection is done by internal circuit using the relationship of YUVHS and YUVVS. 1: Field indication signal is fed from Pin 146 YUVODD (shared with IBGRN3)	0

INCTR3 (Input ConTrol Register 3, 07H)			**Default**
7	USE_IHREF	H active definition for video input pixel data. 0: Use external HREF pin for H active reference. 1: Use internal register (programmable via serial bus) for H active reference.	0
6	USE_IVREF	V active definition for video input lines. 0: Use external VREF pin for V active reference. 1: Use internal register (programmable via serial bus) for V active reference.	0
5	IH_INV4FID	Polarity of HS pulse for field identification. 0: normal. 1: inversed.	0
4	IV_INV4FID	Polarity of VS pulse for field identification. 0: normal. 1: inversed.	0
3:1	ICLK_DELAY[2:0]	Programmable delay for ICLK (or IACLK): 000: 0 unit delay, 001: 1 unit delay, 010: 2 units delay, 011: 3 units delay 100: 4 units delay, 101: 5 units delay, 110: 6 units delay, 111: 7 units delay.	000
0	FID_INV_SCALER	Selection of the inversion of Frame Id for scaler. 0: normal, 1: inversed.	0

INCTR4 (Input ConTrol Register 4, 08H)			Default
7	IA_A2PORT	The first input port selection. 0: Port A selects RGB A Bus.	0
6	IB_B2PORT	The second input port selection. (for YUV as well as RGB inputs) 0: Port B selects RGB B Bus.	0
5	ICLKDIV2_EN	The selection of the generation of ICLKdiv2. This bit should be set for single (24-bit) port input (for YUV as well as RGB inputs) 0: Two-port (48-bit) input is selected. 1: One-port (24-bit) input is selected.	0
4	IHVSDECLK A_B	The HS/VS/DE/CLK input pins selection. 0: Selects input A Bus for HS/VS/DE/CLK control signals. 1: Selects input B Bus for HS/VS/DE/CLK control signals.	0
3-1	IBCLK_DEL A Y[2:0]	Programmable delay for IBCLK: 000: 0 unit delay, 001: 1 unit delay, 010: 2 units delay, 011: 3 units delay 100: 4 units delay, 101: 5 units delay, 110: 6 units delay, 111: 7 units delay.	000
0	FORCE_UP_DN	The direction of deinterlacing is forced or not 0: not forced (all directions are allowed). 1: the direction of deinterlacing is forced to be up and down	0

OUTCTR3 (OUTput ConTrol Register 3, 09H)			Default
7-6	FID32_CLA MP[1:0]	The Clamp pin will send the following signals out. 00: CLAMP signal. 01: FID (Frame Id) signal. 10: Reserved. 11: PWMR0.	00
5	PCLKEQICLK	PCLK source selections: 0: PCLK is from PCLK PLL or external pin PCLK_IN. 1: PCLK is from ICLK. (Normally for 1:1 scaling)	0
4	NTSC_HDTV	Select NTSC or HDTV mode in matrix block 0 : NTSC 1 : HDTV	0
3	RST_GT_AD R	Reload Gamma Table starting address control bit The Gamma Table starting address is reloaded to the value defined by Reg GCSTART (B9h)while there is a low to high transition	0
2	H_FLIP	H-flip activation 0: H-flip is off. 1: H-flip is on (the preset value of the down counter, H_FLIP_COUNT, should be set before this operation.)	0

1	MPWR0ACT	PWM R0 (shared with PRED0 pin) is activated: 0: PRED0 in normal mode. 1: PRED0 will send out the PWM signal. Note: PWMR0 can be also available at CLAMP pin if FID32_CLAMP[1:0] =11.	0
0	MPWB0ACT	PWM B0 (shared with PBLU0 pin) is activated: 0: PBLU0 in normal mode. 1: PBLU0 will send out the PWM signal.	0

MISCTR0 (Misc. ConTrol Register 0, 0AH) (This register can be read and write)			**Default**
7	GAMMAUSE	Use GAMMA correction table for each R,G, and B. 0: Bypass the GAMMA table 1: Use the GAMMA look-up table	0
6	DEINT_OFF_IF_32PD	Deinterlace circuit On/Off control 0: Deinterlace circuit On/Off is fully controlled by the DEINTERLACE_AUTO[1:0] bits at OUTCTR2 (0x05) Register. 1: Reserved.	0
5	VHSYN_SEL	Port A VS & HS synchronization edge 0: Use ACLK rising edge 1: Use ACLK falling edge	0
4	FREEZE	0: Normal function 1: Freeze function	0
3	EOSD_EN	0: External OSD will be disabled 1: External OSD will be enabled (The internal OSD can be enabled by IOSD_EN in bit 0 of OSDCTR1 register)	0
2	EOSDFR	In case of EOSD_EN (bit 3) = 1, 0: Internal OSD will be put in front of external OSD 1: External OSD will be put in front of internal OSD	0
1	BYPASS(Output Free-Run Mode)	0: (default) Panel VS and HS (PVS & PHS) free-runs and acts as a sync master.(In this mode, by programming the FBC_BYPASS bit in FBCTR2 Register, this chip can work with Frame Buffer which does frame rate conversion or free-run for OSD display.) 1: In this mode, the input and output frames are synchronized. In a sense, IVS& IHS are the sync master that generate PVS & PHS. (This chip works without Frame Buffer.) Note: In order to activate free-run mode, micro-controller should choose BYPASS = 0. To this, the input data can be ignored, if necessary, by setting BKFRC= 1 so background colors are sent to panel.	0

0	DE_DIM_EN	Dim of an area (defined by DMH_START, DMH_END, DMV_START, and DMV_END) in the display is enabled if this bit is set	0

MISCTR1 (Misc. ConTrol Register 1, 0B hex)			**Default**
7	MATRIX_ON	The color space conversion (YUV to RGB) matrix is used or bypassed. 0: Bypassed. 1: Used Note: Hue_sat_adjust (bit 5 of 05hex) is used to select hue/satuate or brightness/contrast adjustment.	0
6	Reserved		0
5:4	DITHER_RNG(1:0)	DITHER RNG ON and choices. 00: RNG off 01: RNG 10 10: RNG 12 11: RNG 16	00
3	EOSD_SYNSEL	0: EOSD data latch uses OVCLK 1: EOSD data latch uses the inverse of OVCLK	0

MISCTR1 (Misc. ConTrol Register 1, 0B hex)			**Default**
2	CLAMP_OFF	CLAMP pulse will be generated according to the register 7A and 7B (hex) 0: clamp pulse is sent out. 1: clamp pin is in tri-state	0
1	BACLK_SE L	BACLK_SEL is for IBCLK or IACLK selection. 0: ICLK = IBCLK/2 (for LLC2) 1: ICLK = IACLK	1
0	IIC_ACT_DIRECT	0: 2-wire serial bus parameters are activated until next VS retrace period. 1: 2-wire serial bus parameters are activated upon data received	1

STATUS1 (status Register 0, 0DH) (read only)			**Default**	**RD/WR**
7	reserved			R
6	reserved			R
5-4	reserved			
3	AFREEZE_RDY	For auto adjustment, this status bit will be set to 1 as the freeze function is completed. This is a RD only status bit.		R

2	APXL_REPORT	For auto adjustment, by setting to 0, the PXL_REPORT function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit. The PXL_REPORT function can read the pixel value via PXL_Value (x74 ~ x76) of specified postion via PXL_Address (x9A ~ 9D).		R/W
1	ASOD_RDY	For auto adjustment, by setting to 0, the SOD (sum or sum of difference) function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit.	1	R/W
0	AML_RDY	For auto adjustment, by setting to 0, the Mth line function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit.	1	R/W

INTCTR (Interrupt Control Register, 0EH)			**Default**
7	INTEN	0: Disable all interrupt 1: Enable all interrupt	1
6:0	Reserved		

MISCTR2 (MISC Control Register 2, 0FH)			**Default**
7-5	OVCLK_DELAY[2:0]	OVCLK phase deviation for the nominal clock reference phase . OVCLK_DELAY[2]: 0: OVCLK for OSD output is not inverted, 1: OVCLK for OSD output is inverted. Besides, there are delays defined by OVCLK_DELAY[1:0] as follows: OVCLK_DELAY[1:0]: 00: 0 unit delay, 01: 1 unit delay, 10: 2 units delay, 11: 3 units delay.	000
4-3	DITHER_RNG_RESET[1:0]	RNG reset selection when dithering is used. 00: No reset at all after system power-on reset. 01: RNG reset every VS. 10: RNG reset every 4 VS. 11: RNG reset every 16 VS. NOTE: Programming of RNG or FDBK_ON (feedback path is connected) can be found at OUTCTR2 and MISCTR1.	00
2	VIDEO_FREERUN	Free run of video mode. 0: The VS of panel is synchronized by input video VS. 1: The VS of panel is generated by free running.	0

1	DITHER_TIME	Dithering at spatial or time domain. 0: Dithering will be performed in spatial domain. Programming of RNG or FDBK_ON (feedback path is connected) can be found at OUTCTR2 and MISCTR1. 1: Dithering will be performed in time domain.	0
0	RGB12_DE_DELAY	During the RGB 12 bits input mode, the 12-bit data bus is clocked by the positive or negative edge. This implies the DE is delayed (or not) comparing the corresponding data bus. 0: DE has no delay. 1: DE delayed.	0

INCTR5 (Input Control Register 5, 1FH)			**Default**
7:6	I_DITHER_ON(1:0)	00: no dithering operation for FBC input 01: reserved. 10: 2 bit dithering at special domain for each R/G/B 11: 3 bit dithering at special domain for each R/G/B	00
5:4	I_DITHER_RNG(1:0)	Dithering operation for FBC input with RNG on and choices of cycling. 00: RNG off 01: RNG 10 10: RNG 12 11: RNG 16	00
3	I_DITHER_FDBK_ON	The error due to resolution change is fed back for dithering operation to FBC input 0: feedback path is disconnected. 1: feedback path is connected for dithering.	0

INCTR5 (Input ConTrol Register 5, 1FH)			**Default**
2:1	HMD_VF_CNT[1:0]	HMD (Hardware Mode Detection): V Sync frame count selection 00: Not allowed. 01: (default) VS frame count is 1. 10: VS frame count is 2. 11: VS frame count is 3.	01
0	HS_EQ_HREF	The generation of internal HS signal for video display. 0: Internal HS is different from HREF input.	0

REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE hex	R/W	Description
Input Horizontal Active Start(IH_ASTART[10:0])	11, 10	01,28	W	This value should be at least larger than six.
Input Horizontal Active Width (IH_AWIDTH[11:0])	13, 12	04,00	W	All default values are setting for 1024*768@60Hz
Input Hsync TOTAL (IH_TOTAL[11:0])	15,14	05,40	W	
Input Vertical Active Start (IV_ASTART[10:0])	17,16	00,23	W	
Input Vertical Active Width (IV_AWIDTH[10:0])	19,18	03,00	W	
Input Vsync TOTAL (IV_TOTAL[10:0])	1B,1A	03,26	W	
Input Hsync Pulse Width (IH_PULW[7:0])	1C	**44**	W	This register specifies the pulse width of the input Hsync. Within this region the input video data are forced to zero by the internal circuit. The max. allowed value is 255 (in the unit of iclk).
Input VREF and HREF Delay (IVHREF_DELAY[7:0])	1D	00	W	The H and V delay for YUV input. The MSB 4-bit is defined as. VREF_DELAY[3:0] and the LSB 4-bit is HREF_DELAY[3:0]. By programming this byte, the display of video YUV signals have VREF_DELAY*2 lines and HREF_DELAY*4 pixels offsets in V and H respectively. In a word, the unit of VREF delay is 2*H-line and the unit of HREF delay is 4 pixels (or 6.75MHz). For VREF delay, VREF_DELAY=00 (default) means no delay. For HREF delay, HREF_DELAY=00 (default) means no delay.

REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE hex	R/W	Description
Input VS Delay (VS_EQ_VREF, IVS_DELAY[3:0])	1E	00	W	The input VS delay. The LSB 4-bit is used. By programming these bits, the input VS signal will be delayed by IVS_DELAY*16 or IVS_DELAY*32 pixels (depends on IRGB24=1 or 0, see INCTR1 at register 02H). IVS_DELAY=00 (default) means no delay. The bit higher than IVS_DELAY[3:0] is used for VS_EQ_VREF. Or the generation of internal VS signal for video display. 0: (default) Internal VS is different from VREF input. 1: Internal VS is equal to VREF input.
Registers 1F is used for Input Control Register 5 (INCTR5). Registers 20-2F are described at Auto Adjustment Registers				
Input Vsync Delay for Wrap Around (IV_DELAY4WRAP[10:0])	7D,7C	00,02	W	The V delay for VGA input. The value 2 (default) means no delay and 3 means one H line delay, and so on (0 and 1 are not allowed.)
Input Hsync Delay for Wrap Around (IH_DELAY4WRAP[10:0])	7F,7E	00,01	W	The H delay for VGA input. The value 1 (default) means no delay and 2 means one pixel delay, and so on (0 is not allowed.)
OUTPUT WINDOW PARAMETER				
Panel Horizontal Active Start(PH_ASTART[10:0])	31,30	01,28	W	Please refer to the figure of Output Window
Panel Horizontal Active Width(PH_AWIDTH[10:0])	33,32	04,00	W	
Peaking Control LSB(PEAKING[7:0])	34	00	W	bit[7:4]: select high-pass mode (0~15) for PEAKING bit[3:0]: select band-pass mode (0~15) for both PEAKING and LPF

Peaking Control MSB(PEAKING_ENTER])	35	00	W	bit[1]: whether bypass peaking 0 : enable PEAKING function 1 : BYPASS bit[0]: select low-pass filter or peaking 0 : low pass filter 1 : peaking
Panel Vertical Active Width (PV_AWIDTH[10:0])	37,36	03,00	W	
Panel Vsync EVEN TOTAL (PV_TOTAL_EVEN[10:0])	39,38	03,26	W	This 10-bit register defines the Panel Vertical Active Total Lines for non- interlaced video or the Even Field Active Total Lines for interlaced video.
Panel Hsync Pulse Width(PH_PULW[7:0])	3A	88	W	
Panel Vsync Pulse Width (PV_PULW[7:0])	3B	06		
OLHNVL[10:0]	3D,3C		R	report the offset between the last PHS to next PVS; MSB:x3D[2:0]; LSB:x3C[7:0]
GRAPHIC_START(OSD)	3E	FF	W	Graphic font starting
GRAPHIC_END(OSD)	3F	FF		Graphic font ending
BACKGROUND AND DE DIM WINDOW PARAMETER				
Background Horizontal Start (BH_START[10:0])	41,40	01,28	W	Please refer to the figure of Output Window
Background Horizontal End (BH_END[10:0])	43,42	05,28	W	ALL default values are setting for 1024*768@60Hz
RESERVED	44		W	
RESET_PWM[3:0]	45	03	W	x45[0] : RESET_FBC reset FBC x45[1] : RESET_SCALER reset the rest of blocks (except I2C, PWM, HMD) x45[2] : PWM_OUT_EN 0 : PWM output is enable 1 : PWM output is disable x45[3] : OUTPUT_SWAP 1 : Swap the A/B port output

PV_COMP	47,46	03,FF	W	This register is used to fine tune the PH_TOTAL. When PV_COMP[11] = 1, the fine tune process is turned on. Besides, when the Line Count > PV_COMP[10:0] , the PHS is generated by PH_TOTAL + 1 (single port out) or PH_TOTAL + 2 (dual port out)
DE_DIM Horizontal Start (DMH_START[10:0])	49,48	00,00	W	This parameter is used if DE_DIM_EN is on. The start and end points are counted from the H or V display (background color) region. Please refer to the figure of output Window. ALL default values are set for 1024*768. The MSB 4-bit of 4F, 4E register will be used for the lightness control of DE dim function under the condition that DE_DIM_EN (Bit 0 of MISCTR0) is on. DE_LIGHT[15:12] is used to adjust the contrast of the dim area.
DE_DIM Horizontal End (DMH_END[10:0])	4B,4A	04,00	W	
DE_DIM Vertical Start (DMV_START[10:0])	4D,4C	00,00	W	
DE_DIM Vertical END (DMV_END[10:0]) DE_LIGHT[15:12]	4F, 4E	03,00	W	

PANEL BACKGROUND PARAMETER

Panel background active offset for even field (PB_LEAD_LAG_EN, PBV_AOFFSET_EVEN[9:0])	51, 50	00,00	W	The LSB 10-bit defines the offset of panel background active region for even field. The value is counted from the PV_ASTART. The MSB, PB_LEAD_LAG_EN, defines lead or lag to PV_ASTART.PB_LEAD_LAG_EN = 1 is lag, otherwise (default) lead.
Panel background active offset for odd field (PB_LEAD_LAG_OD, PBV_AOFFSET_ODD[9:0])	53, 52	00,00	W	The LSB 10-bit defines the offset of panel background active region for odd field. The value is counted from the PV_ASTART. The MSB, PB_LEAD_LAG_OD, defines lead or lag to PV_ASTART.PB_LEAD_LAG_OD = 1 is lag, otherwise (default) lead.

Panel background active width (PBV_AWIDTH[10:0])	55, 54	00,00	W	The LSB 11-bit defines the width of panel background active region.
OSD Font address [5:0]	56	00	W	Font RAM write address (auto increment). There are 63 (0x00 ~ 0x3E) address for the downloadable fonts. 0xFF locates the space code.
OSD FONT LSB [7:0]	57	00	W	Font LSB, each font is composed of 20x12 bits
OSD FONT MSB [11:8]	58	00	W	Font MSB
OSD attribute for FONT Code(OSD_AT[7:0])	59	00	W	Font code attribute
OSD FONT code address(OSD_DT[7:0])	5A	00	W	Font code
OSD Display RAM address LSB(0~255)(OSD_ADL[7:0])	5B	00	W	Display RAM, low address range (0-255)
OSD Display RAM address MSB(256-511)(OSD_ADM[7:0])	5C	00	W	Display RAM, high address range (256-511)
OSD System Control	C2	00	W	Bit0~bit1:bits for dot rate selection 00,01: divided by 1 02: divided by 2 03: divided by 3 Bit2:Vint enable interrupt signal to MCU Bit3:WinFB_Ndrive pin FB 0 or 1 Bit5:VintOrEndL selection between the leading edge of Vsync and the last scanning line Bit6:faderate determine the fade rate 0:0.5 sec 1:0.25 sec Bit7:WinMask determine whether the outer of OSD window is displayed (WinMask=0) or not(WinMsk=1).
OSD default setting for space code color (OSD_SPDEF[3:0])	CA	00	W	Bit0:intensity color of space code Bit1:blue color of space code Bit2:green color of space code Bit3:red color of space code Bit5~bit4:Veritical position step Bit7~bit6:Horziontal position step

OSD first display ROW(OSD_SROW[3:0])	CB	00	W	Point to the first display row in the display RAM
OSD Horizontal Start in Window(OSD_HPOS[7:0])	CC	FF	W	The horizontal starting position
OSD Vertical Start in Window(OSD_VPOS[7:0])	CD	FF	W	The vertical starting position
OSD control register2 (OSD_CTRL2)	CE	01	W	Bit0:intensity color of monitor mode Bit1:blue color of monitor mode Bit2:green color of monitor mode Bit3:red color of monitor mode Bit4:NOT used Bit5:wipe enable bit Bit6:wipe In/Out Bit7:wipe direction
OSD control register (OSD_CTRL)	CF	1C	W	Bit0:OSD enable bit Bit1:select blinking rarte Bit2:the polarity of R,G,B,I,FB Bit3:Vsync polarity Bit4:Hysnc polarity Bit5:monitor mode enable Bit6:half-tone/see through-effect enable bit Bit7:determine if background color can be spilt.
PWM_HIGH_PERIOD[15:8]	5D	00	W	Define the duty ratio of PWM. Duty Ratio = PWM_HIGH_PERIOD / PWM_PERIOD Note: MSB should be programed first. LSB is located at x79[7:0]. The smallest value of PWM_HIGH_PERIOD is '1'.
PWM_PERIOD[15:0]	5F,5E	00,FF	W	Define the freqnency of PWM. PWM frequency = 14.318MHz/ 4 /PWM_PREIOD Note: MSB should be programmed first. PWM_PERIOD should be greater than PWM _HIGH_PERIOD. So this PWM can be programed from 55Hz to1.7MHz.

V_LINE_DROP[9:0]	61,60	00,00	W	Number of lines will be dropped for V scaling down with SDRAM. The lines of dropped is defined by (1024-V_LINE_DROP)/1024 =(IV_AWIDTH – Number of dropped lines) / IV_AWIDTH For V scaling down with SDRAM, this register should be set to 0.
Emulated IH period by PCLK(SIH_EMU[12:0])	63,62	05,40	W	The period of pseudo input HS counted by panel clock This value is calculated by PH_TOTAL * SV_NUME / SV_DENO
H_FLIP_COUNT[12:0]	65,64	03,FF	W	Preset value of H-flip down counter. This counter will be activated only if the flag H_FLIP at bit 2 of Reg OUTCTR3 is on.
SHdx[6:0],SHdy[6:0],SHhinc[5:0]	66,67,68	01,00,20	W	SHhinc= floor(32/Hsf), Hdy/Hdx = 32/Hsf - SHhinc. Note that we should set SHdx[5:0]=01, SHdy[5:0]=00, and SHhinc[4:0]=20 for scaling down operation
SVdx[5:0],SVdy[5:0],SVhinc[5:0]	69,6A,6B	01,00,20	W	SVhinc= floor(32/Vsf), Vdy/Vdx= 32/Vsf - SVhinc. These parameters are used for both scaling up and down
SAHdx[6:0], SAHdy[6:0], SDnAHhinc[7:0] (SAHdx[6:0] and SAHdy[6:0] are not used in t0911/t0944/t0946/t0947/t0949/t0959)	6C,6D 6E	01,00,80	W	AHhinc= floor(8*Hsf), AHdy/AHdx= 8*Hsf - AHhinc. The MSB 2-bit of SDnAHhinc is defined as SALGO for scaling algorithm selection, where SALGO = 0 chooses linear interpolation, SALGO = 1 selects bell shape interpolation, SALGO = 2 selects SINC (default), SALGO = 3 chooses pixel replicate. The algorithms in the order of smoothness to sharpness are SINC, bell, linear, and replicate.

				The 3rd and 4th MSB bits of SDnAHhinc, namely **V_SD_ON** and **H_SD_ON**, are used for enabling V and H scaledown operations, i.e. SD_ON=0 (default) for scaling up, SD_ON=1 for scaling down.
Vertical Nume(SV_NUME[5:0])	6F	01	W	Vnume/Vdeno = Vsf (scaling factor in V direction). The Vnume and Vdeno can be any values for scaling up but should be constrained by Vdeno=Vnume + 1 for scaling down.
Vertical Deno(SV_DENO[5:0])	70	01	W	
SDNHdx[5:0],SDNHdy[5:0],SDNHhinc[3:0]	71,72,73	01,00,08	W	For scaling down, SDNHhinc= floor(8/Hsf), SDNHdy/SDNHdx= 8/Hsf - SDNHhinc. Note that we should set SHdx[6:0]=01, SHdy[6:0]=00, and SHhinc[5:0]=20 for scaling down operation. Also note that SDNHdx[5:0]=01, SDNHdy[5:0]=00, and SDNHhinc[3:0] =08 should be set for scaling up operation.
Registers 74-78 are for Auto Adjustments				
MISC				
PWM_HIGH_PERIOD [7:0] (The other two PWMs are located at FE and FF)	79	00	W	Define the duty ratio of PWM. Duty Ratio = PWM_HIGH_PERIOD / PWM_PERIOD Note: should program MSB byte first MSB is located at x5D[7:0]. See also Registers FE-FF for PWMR0 and PWMB0.
Clamp pulse starting setting register (CLAMP_STA)	7A	8A	W	The starting point of clamp pulse setting. Counted from the falling edge of sync pulse by IACLK.
Clamp pulse width setting register (CLAMP_WIDTH)	7B	80	W	The width of clamp pulse by IACLK (1.2us is suggested)

The 1st line of the window for SOD calculation (AWV1START[10:0])	21,20	00,00	W	Define the range of intra-frame SOD operation. Note that AWVSTART and AWHSTART are counted from the starting edge of input VSync/HSync pulse. AWVSTART should be larger than 3 and AWHSTART should be larger than 6.
The last line of the window for SOD calculation (AWV1END[10:0])	23,22	00,00	W	
The 1st pixel of the window for SOD calculation (AWH1START[10:0])	25,24	00,00	W	
The last pixel of the window for SOD calculation (AWH1END[10:0])	27,26	00,00	W	
The 1st line of the window for SOD calculation (AWV2START[10:0])	DD,DC	00,00	W	Define the range of intra-frame SOD operation. Note that AWVSTART and AWHSTART are counted from the starting edge of input VSync/HSync pulse. AWVSTART should be larger than 3 and AWHSTART should be larger than 6.
The last line of the window for SOD calculation (AWV2END[10:0])	DF,DE	00,00	W	
The 1st pixel of the window for SOD calculation (AWH2START[10:0])	FB,FA	00,00	W	
The last pixel of the window for SOD calculation (AWH2END[10:0])	FD,FC	00,00	W	
The resulting value of the sum of the SOD calculation (ASUM[31:0])	28,29, 2A,2B	00,00	R	
The resulting value of sum of difference of the SOD calculation (ASOD[31:0])	2C,2D2E ,2F	00,00	R	
PXL Value	76,75,74	00,00	R	Report the data value of specified position in PXL_Address (x9A~9D) 74 : R 75 : G 76 : B
Reserved	77	00	W	
SOD Mask Register (SODMASK[7:0])	78	00	W	The MSB 3 bit of SODMASK[7:0], SOD_MASK_BIT[2:0], is used to select the number of MSB bits for SOD operation. There are five possibilities. If SOD_MASK_BIT=000, all bits are calculated. If SOD_MASK_BIT=001, the LSB 1 bit is not cared. While if SOD_MASK_BIT=1xx, the LSB4 bits are not cared. The LSB 3 bit of

				SODMASK[7:0], SOD_R_MASK, SOD_G_MASK, and SOD_B_MASK, are used to select the color channels for SOD operation, e.g. if SOD_R_MASK=1, the RED channel is not involved in the calculation. The default state is all channels are calculated.
Registers 79-7B (PWM and clamp) are described at MISC, and Registers 7C-7F (IHV_DELAY4WRAP) are described at INPUT WINDOW.				
Maximum Threshold (ARGB_MAX[7:0])	80	7F	W	Designate the threshold value for R, G, and B. The result will be available at AML_OVERFLOW (Reg. 0xAC)
Minimum Threshold (ARGB_MIN[7:0])	81	00	W	Designate the threshold value for either R, G, or B
Freeze line address(AFZLADDR[10:0])	83,82	00,00	W	Designate the line to be frozen and read by host. The line number is counted from V active region.
Freeze line pixel start address (AFZHSTART[10:0])	85,84	00,00	W	Designate the line to be frozen and read by host. The pixel number is counted from H active region. Please refer to the MSB of OUTCTR0 register 03 Hex
Freeze line read address (AFZREAD[7:0])	86	00	R	After the registers AFZLADDR and AFZHSTART are designated, this register can be read sequentially for the content of frozen line buffer.
The Mth line chosen to check the horizontal start & end (AMLNUM[10:0])	89,88	00,00	R/W	Designated by host, the auto adjust function searches (horizontally) the starting and ending pixels along the Mth line. If 00 are programmed, the entire screen is covered for H_start and H_end points searching.
The 1st line exceeds ARGB_MIN (AVSTART[10:0])	8B,8A	00,00	R	

The last line exceeds ARGB_MIN (AVEND[10:0])	8D,8C	00,00	R	
The 1st pixel exceeds ARGB_MIN position at Mth line (AMLHSTA[10:0])	8F,8E	00,00	R	
The last pixel of the Mth line exceeds ARGB_MIN position (AMLHEND[10:0])	91,90	00,00	R	If SOD_INTRA = 1 (SOD, sum of difference), the number read should minus one.
The RGB value of the 1st pixel of the Mth line that exceeds ARGB_MIN (AMLHSTAR[7:0],AMLHSTAG[7:0],AML HSTAB[7:0])	92,93,94	00,00,00	R	If SOD_INTRA = 1 (SOD, sum of difference), the values are not available.
The RGB value of the last pixel of the Mth line that exceeds ARGB_MIN (AMLHENDR[7:0],AMLHENDG[7:0],AMLHENDB[7:0])	95,96,97	00,00,00	R	f SOD_INTRA = 1 (SOD, sum of difference), the values are not available
RESERVED	98		W	
VHPERLOW_16BIT	99	00		The MSB 4-bit of Reg 99 is Vperiod[3:0] and the LSB 4-bit is Hperiod[3:0]
PXL Address	9B,9A 9D,9C		W	The PXL_REPORT function (xOD[2]) can read the pixel value via PXL_Value (x74 ~ x76) of specified postion via PXL_Address (x9A ~ 9D). Note: 9A 9B V position(Y) 9C 9D H position(X) The position are counted and aligned to V/Hsync.
VSEP_SPT	9F,9E	00,60	R	programmable sampling point , this is a 12-bits register for Csync separation
Registers A0-A7 are for ICLK/PCLK Measurement				
RESERVED	A8		R	
PX_AS_ALINE[3:0]	A9	02	W	The threshold of number of pixels that will be treated as an active line. The LSB 4-bit will be used. The default number is at least 2 pixels will be treated as an active line.

H START point for AUTO ADJUST compare (AH_START[10:0])	AB, AA	00,10	W	The leading edge of searching window (counted from the leading edge of sync pulse). The trailing edge is 2 pixels before the next sync pulse. The value AH_START should be at least larger than six.
An overflow had been detected on the Mth line (AML_OVERFLOW) (0: B channel, 1: G channel, 2: R channel, other bits are reserved)	AC	00	R	An overflow (a value larger or equal to ARGB_MAX[7:0] at Reg 0x80) of color value in R, G, or B has been detected on Mth line
ICLK/PCLK MEASURE PARAMETER				
ICLK MEASURE (XPULSE_BY_ICLK[15:0])	A1,A0	00,00	R	The number the XTAL pulse (programmable at the length of 1K, 2K, 3K,and 4K) counted by the ICLK. Using this measurement, the period of ICLK can be derived by 69.8413*1024* XTAL_ PULSE_SEL /XPULSE_BY_ICLK where XTAL_PULSE_SEL (=1, 2, 3, or 4) is defined in Register INCTR2 (06 hex)
PCLK MEASURE (XPULSE_BY_PCLK[15:0])	A3,A2	00,00	R	The number the XTAL pulse (programmable at the length of 1K, 2K, 3K,and 4K) counted by the PCLK. Using this measurement, the period of PCLK can be derived by 69.8413*1024*XTAL_PULSE_SEL / XPULSE_BY_PCLK where XTAL_PULSE_SEL (=1, 2, 3, or 4) is defined in Register INCTR2 (06 hex)
IH_TOTAL MEASURE (IHTOTAL_BY_ICLK[10:0])	A5,A4	00,00	R	The length of HS period, IH_TOTAL, counted by the ICLK.

MCLK MEASURE (XPULSE_BY_MCLK[15:0])	A7,A6	00,00	R	The number the XTAL pulse (programmable at the length of 1K, 2K, 3K,and 4K) counted by the MCLK.
RCONTRAST[7:0]	AE	00	W	256 level contrast control for R The input signal is multiplied by a value ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0].
RBRIGHTNESS[7:0]	AF	00	W	256 level brightness control for R 7f ->127,..., 01 -> 1, 00 -> 0, ff ->-1,..., 80 -> -128 i.e. The input data is added by a 2,s complement value.
GCONTRAST[7:0]	B0	00	W	256 level contrast control for G
GBRIGHTNESS[7:0]	B1	00	W	256 level brightness control for G
GAMMA table R write Address (GRWADDR[7:0])	B2	00	W	Each gamma-correction table is a 256x10 LUT (look-up table) which can be updated by writing to these ports. Each entity is composed of high and low bytes which share the same write address. Low byte content is written followed by the high byte content. Lower entity data are sent to a certain channel (e.g. R or G or B) followed by the next higher entity. In a word, R channel is updated by sending data for entity 0, 1, till the final one entity255. Then channel G followed by channel B.
GAMMA table G write Address (GGWADDR[7:0])	B3	00	W	
GAMMA table B write Address (GBWADDR[7:0]) (The table write address will be auto increased upon each writing)	B4	00	W	

CLUT write address (CLUTWADDR[7:0])	B5	00	W	The 16x16 Color LUT can be written by host from this port. First the lower byte data are sent to an entity, then followed by the higher byte data, color index 0 is filled followed by color index 1 until color index 15, the final one. The 16-bit output of this color LUT will be interpreted as the RGB565 format, i.e. the MSB 5 bits are for R, the middle 6 bits for G, and the LSB 5 bits for B.
CLUT alpha blending (CLUT_ALPHA[3:0])	B6	00	W	The MSB of CLUT_ALPHA is used indirectly for the interpretation of the I signal of OSD, while CLUT_ALPHA[2:0] is used to select the blending factor between the output of the CLUT and the output of the dithered video. CLUT_ALPHA[3]= 0: The content of CLUT is RGB565. 1: The content of CLUT is RGB555. And the LSB of G will be interpreted as LSB of G of CLUT read out =0: means alpha blending off. =1: means alpha blending on. If alpha blending is on and any one of the internal/external OSD/background color is activated, the final video of panel out will be equal to Video*CLUT_ALPHA[2:0]/8+CLUT* (1-CLUT_ALPHA[2:0]/8). For the case that CLUT_ALPHA[2:0]=0, the final video of panel is directly from the output of CLUT. And for

				CLUT_ALPHA[2:0]=6, the final video is Video*6/8+CLUT*2/8.
BCONTRAST[7:0]	B7	00	W	256 level contrast control for B The input signal is multiplied by a value ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0].
BBRIGHTNESS[7:0]	B8	00	W	256 level brightness control for B 7f->127,..., 01 -> 1, 00 -> 0, ff -> -1,..., 80-> -128 i.e. The input data is added by a 2,s complement value
GCSTART[7:0]	B9	00		Define Gamma Table Starting Address
PLL program parameter				
Registers 0xBA- 0xBE, please refer to the Section of Clock System for PPLL and MPLL setting.				
HMD				
DE_DUMMY_CNT	BF		W	
DE PARAMETER				
DE counts per Vactive (DEno_perV[10:0])	C1,C0	00,00	R	The number of DE pulses per VS period.
IN/OUT HS/VS PARAMETER				
Panel Vertical back-porch (PV_BACKPORCH[7:0])	C3	FF	W	The register defines the back-porch of panel output. This setting is used only when FBC is not bypassed.
Panel HSync total (PH_TOTAL[10:0])	C5,C4	00,00	W	The LSB 11-bit defines the total value of LCD panel HS. The value is counted by PCLK. Using the results of ICLK/PCLK measurement (see Reg. A0-A3), this parameter can be calculated via IH_TOTAL * ICLK_Period = Vsf * PH_TOTAL * PCLK_Period.
Panel HSync delay (PH_DELAY[10:0])	C7,C6	00,00	W	The LSB 11-bit defines the delay of display output HS from IVS. The value is counted by PCLK.

Input SFDP delay (IV_SFDP[7:0])	C8	00	W	The register defines the value of pixel delay of an internal signal SFDP. The value is counted from the falling edge of input VS by ICLK. This delayed signal is used to synchronize the panel VS.
Input SFDL delay (IV_SFDL[5:0])	C9	01	W	The register defines the value of line delay of an internal signal SFDL. The value is counted from the falling edge of input VS by IHS. This delayed signal is used to synchronize the panel VS.
Registers CA-CF are described in OSD Parameters				
Registers D0-DB are described in Hardware Mode Detection Parameters				

FBCTR0 (FBC control 0, E0H)			
Registers E0-EF are described in Frame Buffer Control Parameters			
7	FILL_PAT (test_pat)	0: no operation 1: Write the pattern (a byte data specified by FBC_PAT or hex E5 register) to SDRAM or SGRAM	0
6	LMR_REQ	0: no op. 1: load SDRAM/SGRAM mode register (should be reset to 0 before normal access of SDRAM)	0
5	VGA_DBUF_MODE	1: DOUBLE BUFFER MODE and force FBC to write the upper space of SDRAM (from BASE_ADDR to boundary limit of SDRAM)	0
4	SC_DBUF_MODE	1: DOUBLE BUFFER MODE and force FBC to read the upper space of SDRAM (from BASE_ADDR to boundary limit of SDRAM)	0
3	DOUBLE_BUF_MODE	De-Frame-Tear Mechanism 1 0 : disable 1 : enable	0
2	SKIP_MODE	De-Frame-Tear Mechanism 2 0 : disable 1 : enable	0
1	DRAM_MODE	Select the configuration of SDRAM 0 : 512Kx2x16 1: 1Mx4x16	0
0	BASE_ADDR[16]	When use SDRAM configuration of 1Mx4x16, treat this bit as the bit 16 of BASE_ADDR which is define by BC_BASE_ADDR (xE6,xE7)	0

FBCTR1 (FBC control register1, E1H)			Default
7	V_flip	0: Vertical flip of screen display is disabled. 1: Vertical flip of screen display is enabled. (Note: V-flip is not supported for double buffering)	0
6:4	REF_CYC	Number of refresh cycle per HS for DRAM refresh request (>=4 suggested or >= 4096 cycles per 64ms) 000: 1 cycles, 001: 2 cycle, 010: 3 cycles, 011: 4 cycles, 100: 5 cycles, 101: 6 cycles, 110: 7 cycle, 111: 8 cycles	000
3:0	REF_RASL	Number of cycles between auto refresh RAS pulse (active low) for DRAM (>=8 suggested) 0000: 16 clocks, 0001: 1 clock, 0010: 2 clocks, 0011: 3 clocks, 0100: 4 clocks, 0101: 5 clocks, 0110: 6 cycle, 0111: 7 clocks 1000: 8 clocks, 1001: 9 clocks, 1010: 10 clocks, 1011: 11 clocks, 1100: 12 clocks, 1101: 13 clocks, 1110: 14 cycle, 1111: 15 clocks	1011

FBCTR2 (FBC control2, E2H)			
7	Freeze_FB	0: the content of the frame buffer is updated by the input signals. 1: the content of the frame buffer is frozen and the input signals will be ignored.	0
6	FBC_BYPASS	0: Frame buffer controller will be activated 1: Frame buffer controller will be bypassed and put to power saving mode (turn off MCLK) .	0
5:4	JPEG_MODE [1:0]	00: JPEG Legacy Mode 10: JPEG Horizontal Auto Increment Mode 11: JPEG Vertical Auto Increment Mode	00
3	Interlace_enable	0: Non-interlace frame-buffer read/write 1: Interlace frame-buffer read/write.	0
2	JPEG_load	JPEG segment data writing action started 0: No action. 1: JPEG data load.	0
1:0	ACKPH[1:0]	Wait cycles of ACK (acknowledge for receiving data) for SD/SGRAM interface. Adjust the timing of FBC to latch SD/SGRAM data. 00: 0 wait cycle, 01: 1 wait cycle, 10: 2 wait cycles 11: 3 wait cycles	01

FBCTR3 (FBC control register3, E3H)			Default
7:4	MCLKIN_DELAY[3:0]	MCLK phase deviation for input clock interface MCLKIN_DELAY[3]: 0: MCLK for data input is not inverted, 1: MCLK for data input is inverted. Besides, there are delays defined by MCLKIN_DELAY[2:0] as follows: MCLKIN_DELAY[2:0]: 000: 0 unit delay, 001: 1 unit delay, 010: 2 units delay, 011: 3 units delay 100: 4 unit delay, 101: 5 units delay, 110: 6 units delay, 111: 7 units delay	0000
3:0	MCLKOUT_DELAY[3:0]	MCLK phase deviation for output clock interface MCLKOUT_DELAY[3]: 0: MCLK for data output is not inverted, 1: MCLK for data output is inverted. Besides, there are delays defined by MCLKOUT_DELAY[2:0] as follows: MCLKOUT_DELAY[2:0]: 000: 0 unit delay, 001: 1 unit delay, 010: 2 units delay, 011: 3 units delay 100: 4 unit delay, 101: 5 units delay, 110: 6 units delay, 111: 7 units delay	0000

FBC_PAT (FBC memory test PATtern, E4H)			Default
7	MPAT_7	A pattern of MPAT_[7:0] will be written to R, G, and B component of frame buffer for memory testing	0
6	MPAT_6		0
5	MPAT_5		0
4	MPAT_4		0
3	MPAT_3		0
2	MPAT_2		0
1	MPAT_1		0
0	MPAT_0		0
A frame buffer test pattern can be defined and tested by the settings in FBC_PAT register (0FH) and the bit 7 (FILL_PAT) of FBCTR0 (07H).			

(FBC E5H)			Default
xE5	FBC_JPEG_HS_NUM	When JPEG_MODE = “10” (Horizontal Auto Increment Mode), set this register to the number of vertical JPEG blocks in one frame.	00

FBC_BASE_ADDR setting (E6, E7 Hex)			Default
E7,E6	Base address of SDRAM addressing space (FBC_BASE_ADDR[15:0])	The registers should be set before the FBC enters into the following three modes: (1) De-frame-tear mode. (2) Double buffer mode (3) Self test mode. The value of FBC_BASE_ADDR is 32 word alignment with respective to the physical SDRAM address, i.e. 5 zeros will be attached to the LSB. For example, set the FBC_BASE_ADDR with 0x0101, the actual address will be 0x02020.	00,00

FBC_1H_TOTAL setting (E9, E8 Hex)			Default
E9,E8	IH Total value for FBC (FBC_IH_TOTAL[15:0])	Depends on the horizontal active width.	02,58

SD/SGDRAM mode setting (EB, EA Hex)			Default
EB,EA	SG/SDRAM mode setting register (FBC_DRAM_MODE[11:0])	The 12-bit data for SG/SDRAM mode setting. xEB[1:0] : Write Burst Mode 0: Programmed Burst Length 1: Single Location Access (default) xEA[6:4] : CAS Latency 010 : CAS Latency 2 (default) 011 : CAS Latency 3 xEA[3] : Burst Type 0 : Sequential (default) 1 : Interleaved xEA[2:0] : Burst Length 000: 1 001: 2 010: 4 011: 8 111: Full Page (default) When you adjust the CAS Latency, you should adjust the setting of register xE2[1:0] to delay the latch SDRAM data timing. After setting the values for this mode register, one should set the LMR_REQ to 1 and then reset it to 0. The LMR_REQ is at bit 6 of FBCTR0 (E0hex)	02,27

SD/SGDRAM refresh setting (ED, EC Hex)			Default
ED,EC	No. of cycles between refresh RAS pulse (SET_REF_IHS,FBC_REF_TIME[11:0])	No. of cycles between refresh RAS (active low) pulse is assigned by the following: The refresh requirement of DRAM is 4096/64ms. If the access clock of SDRAM is 100MHz. The REF_TIME should be less than the value mclk*64*1000/4096 where the unit of mclk is MHz. There is a SET_REF_IHS bit located at the next MSB side of FBC_REF_TIME[11:0]. If the SET_REF_IHS bit is set to one , the generation of SDRAM refresh cycle will be synchronous to input H sync signal or the refresh timer (0xED[11:8], 0xEC[7:0]) expired. If the SET_REF_IHS is 0, the SDRAM refresh cycle will be generated only when the refresh timer (0xED[11:8] , 0xEC[7:0]) expired.	1f,00

FBC_TEST_CN (FBC TEST CONTROL, EEH)			Default
7	FBC_VS	VS signal set and reset for FBC test control	0
6	FBC_VAC	T FBC V-active signal set and reset for FBC test control.	0
5	FBC_HS	FBC HS signal set and reset for FBC test control.	0
4	FBC_HACT	FBC H-active signal set and reset for FBC test control.	0
3	FBC_SDRAM_RD	FBC SDRAM read signal set and reset for FBC test control.	0
2	CLR_MEM	Toggle the bit will clear the SDRAM with the pattern programed by FBC_PAT(xE4). The clear space is selected by CLE_AB_SEL (xEE[1])	0
1	CLR_AB_SEL	This bit will select which buffer to be clear.	0
0	FBC_TEST_ ACT	Activate the SDRAM self-test.	0

FBC_TEST RESULT (EF Hex)			Default
EF	FBC_TEST_RESULT	SD/SGRAM test resulting data (read only)	00

REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE hex	R/W	Description
Register E0-EF are described in Frame Buffer Control Parameters				
Starting address of x direction for JPEG write (JPEG_WR_X[10:0])	F1,F0	00,00	W	The LSB 11-bit defines the starting address of x direction for JPEG write.

Starting address of y direction for JPEG write (JPEG_WR_Y[10:0])	F3,F2	00,00	W	The LSB 11-bit defines the starting address of y direction for JPEG write.
Reserved	F7,F6			
Threshold for motion detection of the deinterlacing circuit (CNMA_THDmotion[15:0])	F9,F8	00,20	W	This 2-byte register is used as the threshold of the motion detection of the de-interlacing circuit. The higher the value, the higher the possibility that the picture sequence will be treated as a static clip.
PWMR0[7:0]	FE	00	W	In ZiproSX, the PWMR0 (pulse width modulated) signal shares the pin with PRED0.The selection is controlled by the PRED0ACT bit 1 in OUTCTR3. The default value 00 means a low output while the value ff (hex) can be integrated by a capacitor for an almost high signal. Note: This signal can also be accessed at CLAMP Pin by setting the bits FID32_CLAMP=11(bin) at OUTCTR3 (0x09) Register.
PWMB0[7:0] (There is another PWM described at Reg. 79)	FF	00	W	In ZiproSX, the PWMB0 (pulse width modulated) signal shares the pin with PBLU0.The selection is controlled by the PBLU0ACT bit 0 in OUTCTR3. The default value 00 means a low output while the value ff (hex) can be integrated by a capacitor for an almost high signal.

Following is the control registers table of the ZiproSX internal OSD. The description of each register is as follows.

Table1 Control Register Table

REGISTER FUNCTION	ADDR (HEX)	Bit Map								Reset Value
		B 7	**B 6**	**B 5**	**B 4**	**B 3**	**B 2**	**B 1**	**B 0**	
OSDAT	59 H	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	00 H
OSDAT	5AH	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	00 H
OSDADL	5BH	A d 7	A d 6	A d 5	A d 4	A d 3	A d 2	A d 1	A d 0	00 H
OSDADH	5CH	A d 7	A d 6	A d 5	A d 4	A d 3	A d 2	A d 1	A d 0	00 H
OSDFAddr	56H	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	00 H
OSDFontL	57H	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	00 H
OSDFontM	58H	-	-	-	-	D 1 1	D 1 0	D 9	D 8	00 H
SysControl	C2 H	W I N M a s k	F a d e r a t e -	V i n t O R E N D L	V L v L	W i n F B _ N	V i n t	C L K m u x 1	C L K m u x 0	00 H

REGISTER FUNCTION	ADDR (HEX)	Bit Map								Reset Value
		B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0	
OSDSP-def	CA H	HPStep1	HPStep0	VPStep1	VPStep0	R	G	B	I	00 H
OSDStartRow	CB H	-	-	-	-	Row3	Row2	Row1	Row0	00 H
OSDHpos	CC H	H7	H6	H5	H4	H3	H2	H1	H0	7F H
OSDVpos	CC H	V7	V6	V5	V4	V3	V2	V1	V0	3F H
OSDCtrl2	CE H	WipeD	WipeIn/Out	WipeEna	-	R	G	B	I	02 H
OSDCtrl	CF H	Split	H-tone	Monitor	Hp	Vp	Bp	Bf	OSDE	1C H

Graphic_Start	3EH	GStart7	GStart76	GStart5	GStart3	GStart33	GStart2	GStart3	GStart0	FFH
Graphic_End	3FH	GEnd7	GEnd6	GEnd5	GEnd4	GEnd3	GEnd2	GEnd1	GEnd0	FFH
OSDWindow_Addr	F4H	-	-	-	-	Addr3	Addr2	Addr1	Addr0	00H
OSDWindow_Data	F5H	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	00H

Table 2 OSD Window Register Table

REGISTER FUNCTION	ADDR (HEX)	Bit Map								Reset Value
		b7	b6	b5	b4	b3	b2	b1	b0	
Win1V	0H	V1min3	V1min2	V1min1	V1min0	V1min3	V1min2	V1min1	V1min0	00H
Win1HS	1H	H1min4	H1min3	H1min2	H1min1	H1min0	H1min	H1mint	H1min	00H

WIn1HE	2H	H1max4	H1max3	H1max2	H1max1	H1max0	H1max	H1max	H1max	00H
Win2V	4H	V2min3	V2min2	V2min1	V2min0	V2min3	V2min2	V2min1	V2min0	00H
Win2HS	5H	H2min4	H2min3	H2min2	H2min1	H2min0	H2min	Hmint	H2min	00H
Win2HE	6H	H2max4	H2max3	H2max2	H2max1	H2max0	H2m2R	H2m2G	H2m2B	00H
Win3V	8H	V3min3	V3min2	V3min1	V3min0	V3min3	V3min2	V3min1	V3min0	00H
Win3HS	9H	H3min4	H3min3	H3min2	H3min1	H3min0	H3min	H3mint	H3min	00H
Win3HE	AH	H3max4	H3max3	H3max2	H3max1	H3max0	H3m3R	H3m3G	H3m3B	00H

Win4V	CH	V4min3	V4min2	V4min1	V4min0	V4max3	V4max2	V4max1	V4max0	00H
Win4HS	DH	H4min4	H4min3	H4min2	H4min1	H4min0	Win4E	Win4HT	Win4I	00H
Win4HE	EH	H4max4	H4max3	H4max2	H4max1	H4max0	Win4r	Win4g	Win4b	00H
Win1SH	3H	W1SHC2	W1SHC1	W1SHC0	W1SHCn	W1SHW1	W1SHW0	W1SHH1	W1SHH0	00H
Win2SH	7H	W2SHC2	W2SHC1	W2SHC0	W2SHOn	W2SHW1	W2SHW0	W2SHH1	W2SHH0	00H
Win3SH	BH	W3SHC2	W3SHC1	W3SHC0	W3SHOn	W3SHW1	W3SHW0	W3SHH1	W3SHH0	00H
WiN4SH	FH	W4SHC2	W4SHC1	W4SHC0	W4SHOn	W4SHW1	W4SHW0	W4SHH1	W4SHH0	00H

OSDFAddr: Font RAM ADDRESS Pointer,
ADDRESS:**56H**
There are 63 locations for Font RAM. The updating or retrieving can be directed to any address by an internal address pointer. Before WRITE or after READ, the address pointer will be increased automatically. Be aware each font site comprises 20 font row. So, every 20 words transaction, the content of OSDFAddr will be increased by one. Note Font code 3FH is reserved as a space code; so the data filled in the location is meaningless.

The OSD fonts can be download to any font address from 00H to 3EH of the font RAM. But when they were read out, the font address should add an offset C0H which is the font number of the font ROM . In other words, when read the font RAM the address is from C0H to FEH.

OSDFontL: The 8 LSB BITS OF FONTROW
ADDRESS:**57H**
This is an entry window to fill the content of FONT RAM. Note every row for each font contains 12 bits. It is meant two data segment, 8 LSB bits of Font row and 4 MSB bits of Font row, will be assembled together before transferred to the FONT RAM.

OSDFontL can be rguarded as the buffer to keep the low nibble (8 bits) data before the complete data (12bits) is transferred to the Font RAM. To read back the low nibble data fron FONT RAM,a read action to OSDFontM must be done first, since a read to OSDFontMis a real trigger to get the complete 12 bits from Font RAM.

OSDFontM: THE 4 MSB BITS OF FONTROW
ADDRESS:**58H**
As mention above, OSDFontM is a buffer to keep the upper nibble (4 bits) data before the complete data (12 bits) is transferred to the Font RAM, READ/WRITE from/to mechanism will cause 8 bits of data stored in OSDFontL assembled together with 4 bits of data received in OSDFontM and then transferred to font RAM.

Meanwhile the internal address pointer will be increased automatically. To read the content of font RAM, a READ to OSDFontM will cause a complete Font RAM word distributed to OSDFontL and OSDFontM .

After that the internal address pointer is increased automatically.

OSDAT: FONT CODE ATTRIBUTE;
ADDRESS: **59 H**
This is an entry window to update the content of the Display RAM. Note every word contains 17 bits. Row Attribute, located at the first column, includes 16 bits. It is meant two data segments, 8 bits of Font Code attribute (for Row Attribute, it stands for 8 low nibble bits; i.e. EOD field, Shadow mode field, Character Width, Character Height fields and the LSB of the field of the programmable character height) and 9 bits of Font code (for Row Attribute, it stands for 8 upper nibble bits), will be assembled together before transferred to the Display RAM.

OSDAT can be regarded as the buffer to keep the low nibble (8 bits) data before the complete data (16 bits for Display Font; 16 bits for Row Attribute) is transferred to the Display RAM. In many occasions, a series of display stream might share the same attribute. For this case, OSDAT is just needed to be written once, and then the attribute stored in this buffer will be cascaded together with upper nibble data (9 bits for Display Font; 8 bits for Row Attribute) to form the complete word for Display RAM.

To read back the attribute or low nibble data from Display RAM, a read action to OSDDT must be done first, since a read to OSDDT is a real trigger to get the complete 16 bits from Display RAM.

OSDDT: FONT CODE (INCLUDING SPACE CODE, FF H),
ADDRESS: **5A H**
As above mentioned, OSDDT is a buffer to keep the 8 bits of Font code or upper nibble (8 bits) of the row attribute data before the complete data is transferred to the Display RAM. In the READ/WRITE mechanism of the Display RAM, READ/WRITE from/to OSDDT is actually a real trigger to start the operation. To update the Display RAM, a WRITE to OSDDT will cause 8 bits of data stored in OSDAT assembled together with of data received in OSDDT and then transferred to Display RAM. Meanwhile, the address pointer will be increased automatically. To read the content of Display RAM, a READ to OSDDT will cause a complete Display RAM word distributed to OSDAT and OSDDT. After that, the address pointer will be increased automatically.

OSDADL: DISPLAY RAM ADDRESS POINTER FOR LOWER PART (0 - 255),
ADDRESS: **5B H**
There are 512 locations for Display RAM. The updating or retrieving can be directed to any address by an internal address pointer. For the low range (address 0 - 255), a WRITE to OSDADL will forward the address directly to the internal address pointer without offset. A READ from OSDADL will get the low nibble (bit 0 to Bit 7) of the internal address pointer.

OSDADH: DISPLAY RAM ADDRESS POINTER FOR UPPER PART (256 -511),
ADDRESS: **5C H**
It is similar to OSDADL. However, this register covers the upper range (address 256 - 511) of the Display RAM. A WRITE to OSDADH will cause the address transferred from serial interface to be added by 256. For instance, if 200 is written to OSDADH, then actually 456 (200+256) will be filled in the internal address pointer. A READ from OSDADH will get the upper nibble (bit 1 to Bit 8) of the internal address pointer.

SYSCONTROL: SYSTEM CONTROL REGISTER ,
ADDRESS: **C2 H**

BITS	MNEMONIC	DESCRIPTION
7	WinMask	Determine whether the outer OSD area of the defined window domain is displayed (WinMask = 0) or not (WinMask = 1)
6	FadeRate	Determine the fade in/out rate, 0.5 sec (FadeRate = 0) or 0.25 sec (FadeRate = 1)
5	VintOrEndL	Selection between the leading edge of Vsync and the last scanning line reached
4	VLVL	Read only bit to indicate the polarity of Vsync
3	WinFB_N	Determine if FB always goes low in Window color rendering
2	Vint	Enable interrupt signal to MCU
1-0	CLKmux1-0	Divider to derive OSDCLK

Note:

1. The clock used for OSD circuitry and Serial interface, fOSD is derived from fPclk as follows: fOSD = fPclk / (CLKMUX)

CLKMUX1	CLKMUX0	CLKMUX
0	0	1
1	0	2
1	1	3

2. If VINT is set, then Intensity pin will not deliver Intensity color. Instead, either a wide pulse indicating the leading edge of Vsync (if VintOrEndL from SystemControl is clear) or a wide pulse highlighting the last scanning line for ending display (if VintOrEndL from SystemControl2 is set; when the last scanning line of the last display row is reached, this signal will be always asserted until Vsync coming), will show on the Intensity pin.

3. When WinFB_N is clear, FB pin deliver High state during Characters/shadow/background or window color display. Otherwise, FB pin will always drive low when window color is displaying.

4. VLVL is a read only bit. Since Vsync is always processed by the positive polarity signal internally. So, if VLVL is set, it is meant Vsync is in fly-back period. Otherwise, Vsync will be in the active stage. This function is associated with Vint bit from SysControl1 so that MCU can monitor the progress of OSD.

5. For VintOrEndL, please refer to Vint

OSDSPDEF: SPACE CODE DEFAULT SETTING,
ADDRESS: **CAH**

BITS	MNEMONI C	DESCRIPTION
7 - 6	HposStep	Horizontal moving resolution: 00 (2 dots), 01 (4 dots), 10 (6 dots), 11 (8 dots)
5 - 4	VposStep	Vertical moving resolution: 00 (2lines), 01 (4 lines), 10 (6 lines), 11 (8 lines)
3	R	Red Color of color index
2	G	Green Color of color index
1	B	Blue Color of color index
0	I	Intensity Color of color index

Note:
1. If SPace code is not present yet, OSDSPdef defines the default color setting for shadow/background color.

OSDSTARTROW: DISPLAY STARTING ROW,
ADDRESS: **CBH**

BITS	MNEMONI C	DESCRIPTION
7 - 6	Not used	Should be kept at 0000
5	G8	MSB of Graphic_Start and Graphic_End
4	D8	MSB of OSDDT
3 - 0	Row3 - Row0	Point to the first display row in the Display RAM

Note:
1. The first row in the Display RAM, which will be mapped to the screen as the top display row, will be defined by OSDStartRow.

OSDHPOS: HORIZONTAL STARTING POSITION OF OSD,
ADDRESS: **CCH**

BITS	MNEMONI C	DESCRIPTION
7 - 0	H7 - H0	The horizontal starting position

Note:

1. The horizontal starting position is calculated as follows:
   Hstart position = (HposStep * OSDHpos + 35)/fOSD OSDHpos > 2
2. In order to have more reliable operation, the horizontal starting position is aligned and counted from the leading edge of Hsync fly-back signal coming from deflection circuit. It is not recommended to program too small value for OSDHpos, since the starting part might be still in the fly-back interval.

OSDVPOS: VERTICAL STARTING POSITION OF OSD,
ADDRESS: **CDH**

BITS	MNEMONI C	DESCRIPTION
7 - 0	V7 - V0	The vertical starting position

Note:

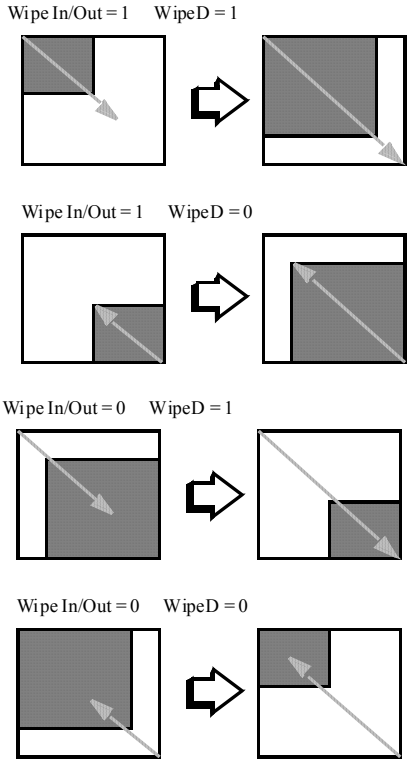
1. The vertical starting position is calculated as follows:
   Vstart position = (VposStep * OSDVpos + 1)/fH
   OSDVpos > 1
2. In order to have more reliable operation, the vertical starting position is aligned and counted from the leading edge of Vsync fly-back signal coming from deflection circuit. It is not recommended to program too small value for OSDVpos, since the starting part might be still in the fly-back interval.

OSDCTRL2: OSD CONTROL REGISTER 2,
ADDRESS: **CEH**

BITS	MNEMONI C	DESCRIPTION
7	WipeD	Determine the direction of Wipe in/out
6	Wipe	In/Out Wipe In or Wipe Out is rendering
5	WipeEna	Wipe In/Out enable bit
4	Not used	Should be kept at 0
3	R	Red color of color index
2	G	Green color of color index
1	B	Blue color of color index
0	I	Intensity color of color index

Note:

1. WipeD, Wipe In/Out, WipeEna flags perform the complete Wipe In or Wipe Out function.
   WipeD: 1 stands for OSD showing up from left-top corner to right-bottom corner; or OSD disappearing from left-top corner to right-bottom corner.
   : 0 stands for OSD showing up from right-bottom corner to left-top corner; or OSD disappearing from right-bottom corner to left-top corner.
   Wipe In/Out: 1 stands for OSD wiping in (OSDE in OSDCtrl must be set beforehand).
   : 0 stands for OSD wiping out (after OSD disappear, OSDE will be clear also).
   WipeEna: 1stands for enabling Wipe In or Out function.
   0 stands for disabling wipe function.
2. In Monitor mode (Monitor bit in OSDCtrl is set), the complete screen will be covered by the color predefined by Bit 0 to Bit3. OSD menu and Windows will be displayed on top of this monitor background color.



Wipe In/Out Operation

OSDCTRL: OSD CONTROL REGISTER ,
ADDRESS: **CFH**

BITS	MNEMONI C	DESCRIPTION
7	Split	Determine if background color can be split
6	Htone	Half-tone/see-through effect enable bit
5	Monitor	Monitor mode enable bit
4	Hp	Hsync Polarity
3	Vp	Vsync Polarity
2	Bp	The Polarity of R, G, B, I and FB
1	Bf	Select the blinking rate
0	OSDE	OSD enable bit

Note:

1. Split bit is valid in boxing mode.
   0: The background color is not split in the midway of SPace code.
   1: The background color is split in the midway of Space code.
2. HalfTone bit is valid in boxing mode.
   0: No see-through effect can be performed in the boxing mode.
   1: The background color will become semi-transparent.
3. Monitor mode selection
   0: Normal mode; Monitor mode is disabled.
   1: Monitor mode is enabled
4. Hp, the polarity of horizontal sync, identified and programmed by MCU
   0: Negative polarity for Hsync.
   1: Positive polarity for Hsync.
5. Vp, the polarity of vertical sync, identified and programmed by MCU
   0: Negative polarity for Vsync.
   1: Positive polarity for Vsync.
6. Bp, the polarity of Red, Green, Blue, Intensity and FB outputs, depending on application needs.
   0: Negative polarity for video outputs.
   1: Positive polarity for video outputs.
7. Bf, the blinking rate selection,
   0: displaying or not displaying toggled per 32Vsync pulses
   1: displaying or not displaying toggled per 64Vsync pulses
8. OSDE, OSD enable bit
   0: OSD disabled; OSDE can be also clear by hardware after Wipe Out is performed
   1: OSD enabled

Graphic_Start: GRAPHIC FONT STARTING,
ADDRESS: **3E H**

BITS	MNEMONI C	DESCRIPTION
7 - 0	Gstart7 - Gstart0	8 LSB bits, associated with Bit 5 in OSDStartRow, defines the starting address of the graphic character font.

Graphic_End: GRAPHIC FONT ENDING,
ADDRESS :**3F H**

BITS	MNEMONI C	DESCRIPTION
7 - 0	Gend7 - Gend0	8 LSB bits, associated with Bit 5 in OSDStartRow, defines the end address of the graphic character font.

Note: The MSB(bit 8) of Gstart and Gend is at register CBH bit 5.

OSDWindow_Addr: OSD WINDOW ADDRESS REGISTER,
ADDRESS: **F4H**

BITS	MNEMONI C	DESCRIPTION
3- 0	Addr3 - Addr0	Address port of the of OSD window register

The ZiproSX OSD support 4 OSD windows and each window was defined by 4 registers. So, there are total 16 registers range from 0H to FH. The indirect addressing mode was used to access the 16 registers.

The OSDWindw_Addr was dedicated as the address port and OSDWindow_Data was dedicated to data port. When user want to program the window's associated registers, they should write a address to address port first and then write the data to data port(F5H). Once the write operation is completed, the internal address pointer will increased by 1 automatically. So, there is no need to program the address port again when continued registers were programmed.

OSDWindow_Data: OSD WINDOW DATA REGISTER,
ADDRESS : **F5H**

BITS	MNEMONI C	DESCRIPTION
7 - 0	Data7 - Data0	Data port of the OSD window register.

This register was the data port when access the OSD window registers. Write data to this register will trigger a write operation to one of the 16 OSD registers selected by the OSDWindow_Addr.

Note: Following 16 OSD window registers was using indirect addressing and should be accessed through the registers F4H and F5H.

WIN1V: VERTICAL RANGE OF WINDOW 1,
ADDRESS: **0 H**

BITS	MNEMONI C	DESCRIPTION
7 - 4	V1MIN3 - V1MIN0	The starting row of Window 1 in the Display RAM
3 - 0	V1MAX3 - V1MAX0	The ending row of Window1 in the Display RAM

WIN1HS: HORIZONTAL STARTING COLUMN OF WINDOW 1,
ADDRESS: **1 H**

BITS	MNEMONI C	DESCRIPTION
7 - 3	H1MIN4 - H1MIN0	The starting column of Window 1 in the Display RAM
2	Win1E	Window 1 enable bit
1	Win1Ht	Window 1 halftone enable bit
0	Win1I	The Intensity color of window color index

Note:

1. If Win1E is set, the Window 1 will be enabled. If more than one Windows are enabled, Window 1 will always have the highest priority.
2. If Win1Ht is set, the Window will become halftone window, which is completely created by the internal circuitry

WIN1HE: HORIZONTAL ENDING COLUMN OF WINDOW 1,
ADDRESS: **2 H**

BITS	MNEMONI C	DESCRIPTION
7 - 3	H1MAX4 - H1MAX0	The ending column of Window 1 in the Display RAM
2	Win1R	The Red color of window color index
1	Win1G	The Green color of window color index
0	Win1B	The Blue color of window color index

WIN2V: VERTICAL RANGE OF WINDOW 2,
ADDRESS: **4 H**

BITS	MNEMONI C	DESCRIPTION
7 - 4	V2MIN3 - V2MIN0	The starting row of Window 2 in the Display RAM
3 - 0	V2MAX3 - V2MAX0	The ending row of Window2 in the Display RAM

WIN2HS: HORIZONTAL STARTING COLUMN OF WINDOW 2,
ADDRESS: **5 H**

BITS	MNEMONI C	DESCRIPTION
7 - 3	H2MIN4 - H2MIN0	The starting column of Window 2 in the Display RAM
2	Win2E	Window 2 enable bit
1	Win2Ht	Window 2 halftone enable bit
0	Win2I	The Intensity color of window color index

Note:

1. If Win2E is set, the Window 2 will be enabled. If more than one Windows are enabled, Window 2 will have the second priority.
2. If Win2Ht is set, the Window will become halftone window, which is completely created by the internal circuitry

WIN2HE: HORIZONTAL ENDING COLUMN OF WINDOW 2,
ADDRESS: **6 H**

BITS	MNEMONI C	DESCRIPTION
7 - 3	H2MAX4 - H2MAX0	The ending column of Window 2 in the Display RAM
2	Win2R	The Red color of window color index
1	Win2G	The Green color of window color index
0	Win2B	The Blue color of window color index

The Window operation is demonstrated in following figure. The original display Row is started at row 4, which is pointed by OSDStartRow, and ended at row 13 (the EOD bit of the row attribute for Row 13 is set). The configuration for registers related to windows is shown in following figure. Some original display data like data in Row4 and Row13 becomes invisible (WinMask bit is set here).

It is very important to know the programmed range for Window 1 and Window 2 must be covered by the original visible domain, defined by OSDStartRow and EOD bit setting for the last display row.

WIN3V: VERTICAL RANGE OF WINDOW 3,
ADDRESS: **8 H**
(Defining the vertical range of window3, for the details, please refer to WIN1V)

WIN3HS: HORIZONTAL STARTING COLUMN OF WINDOW 3,
ADDRESS: **9 H**
(Defining the horizontal starting column of window3, enable bit, Halftone control bit and color intensity it, for the details, please refer to WIN1HS)

WIN3HE: HORIZONTAL ENDINGCOLUMN OF WINDOW 3,
ADDRESS: **A H**
(Defining the horizontal ending column of window3, color R, G, B bits, for the details, please refer to WIN1HE)

WIN4V: Vertical range of Window 4,
ADDRESS: **C H**
(Defining the vertical range of window 4, for the details, please refer to WIN1V)

WIN4HS: Horizontal starting column of Window 4,
ADDRESS: **D H**
(Defining the horizontal starting column of window 4, enable bit, Halftone control bit and color intensity bit, for the details, please refer to WIN1HS)

WIN4HE: Horizontal ending column of Window 4,
ADDRESS: **E H**
(Defining the horizontal ending column of window 4, color R, G, B bits, for the details, please refer to WIN1HE)

WIN1SH:Shadow effect for window 1,
ADDRESS: **3 H**

BITS	MNEMONI C	DESCRIPTION
7 – 5	W1SHC2 - W1SHC0	The color of the window shadow
4	W1SHOn	If set, enable the window shadow if cleared, disable the window shadow
3 – 2	W1SHW1 - W1SHW0	The width of the window shadow
1	W1SHH1 - W1SHH0	The height of the window shadow

Note:
1. The color of the window shadow is encoded as follows:

W1SHC2	W1SHC1	W1SHC0	COLOR
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

2. The shadow width is defined as follows.

W1SHW1	W1SHW0	WIDTH : SHW (IN UNIT OF DOT)
0	0	2
0	1	4
1	0	6
1	1	8

3. The shadow height is defined as follows.

W1SHH1	W1SHH0	WIDTH : SHH (IN UNIT OF LINE)
0	0	2
0	1	4
1	0	6
1	1	8

WIN2SH: Shadow effect for window 2, ADDRESS: **7 H**
(Defining the window shadow of window 2. For the details, please refer toWIN1SH)

WIN3SH: Shadow effect for window 3, ADDRESS: **B H**
(Defining the window shadow of window 3. For the details, please refer to WIN1SH)

WIN4SH: Shadow effect for window 4, ADDRESS: **F H**
(Defining the window shadow of window 4. For the details, please refer to WIN1SH)

Win1V = 8CH (Row 8 to Row 12);
Win1HS = 2CH (Starting Column = 5);
Win1HE = A6H (Ending Column = 20; Yellow)

Win2V = 59H (Row 5 to Row 9);
Win2HS = 1DH (Starting Column = 3);
Win2HE = 69H (Ending Column = 13; Light Blue)

SHH1 = 11; SHH2 = 11
SHW1 = 11; SHW2 = 01

FIGURE 25 .This Figure Show the OSD Window Operation

6.0 REGISTER MAP HARDWARE MODE DETECTOR

TABLE 22. The register map of Hardware Mode Detector

Name: (bit)	7	6	5	4	3	2	1	0
HWDCNT (D0H)	Enhwd	SelDE	Hwd_inten	Vint_ren	Vint_fen	Vcnt- Sel	HVsep1	HVsep 0
83H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IntSrc (D1H)	-	-	Vint_R	Vint_F	VfChanged	Vpolcha	HfChanged	Hpolcha
00H	-	-	R	R	R	R	R	R
SyncStatus (D2H)	-	Falt	FwHalf	Odd_Even	Vpresence	Hpresence	Vpolarity	Hpolarity
00H	-	R	R	R	R	R	R	R
HperHigh (D3H)	Hper11	Hper10	Hper9	Hper8	Hper7	Hper6	Hper5	Hper4
00H	R	R	R	R	R	R	R	R
VhperLow (D4H)	Vper3	Vper2	Vper1	Vper0	Vper3	Vper2	Vper1	Vper0
00H	R	R	R	R	R	R	R	R

TABLE 22. The register map of Hardware Mode Detector

Name: (bit)	7	6	5	4	3	2	1	0
VperHigh (D5H)	Vper11	Vper10	Vper9	Vper8	Vper7	Vper6	Vper5	Vper4
00H	R	R	R	R	R	R	R	R
PulCnt (D6H)	EnVout	EnHout	VoutMode1	VoutMode0	HoutMode1	HoutMode0	Htolerance1	Htolerance0
C0H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVPwth (D7H)	EOEnable	VPW3	VPW2	VPW1	VPW0	HPW2	HPW1	HPW0
43H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PoutPolPos (D8H)	VCoast Delay1	VCoast Delay0	Vshift3	Vshift2	Vshift1	Vshift0	Vout-Pol	Hout-Pol
00H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HfpHigh (D9H)	Hfp9	Hfp8	Hfp7	Hfp6	Hfp5	Hfp4	Hfp3	Hfp2

4AH	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HvfpLow (DAH)	Vtolerance1	Vtolerance0	Vfp3	Vfp2	Vfp1	Vfp0	Hfp1	Hfp0
18H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VfpHigh (DBH)	Vfp11	Vfp10	Vfp9	Vfp8	Vfp7	Vfp6	Vfp5	Vfp4
32H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TABLE 23.

HWDCNT (Hardware Mode Detector Control Register, 0xD0)		
7	Enhwd	Enable Hardware mode detectorEnable 0: Disabled; (clock is sleeping also to save power) 1: Enabled
6	SelDE	Selection between DE and Csync input (DE and Csync are mutually exclusive) (if SelDE = 1, HVsep is automatically set as 00) 0: Csync is selected 1: DE is selected
5	Hwd_inten	Enable interrupt from one of Sync signal changes: H/V frequency or Polarity change 0: Disabled 1: Enabled
4	Vint_ren	Enable interrupt at Vsync leading edge 0: Disabled 1: Enabled
3	Vint_fen	Enable interrupt at Vsync trailing edge 0: Disabled 1: Enabled
2	Vcnt_Sel	Select Vperiod count by time or by line number 0: By time; i.e. Vclk (Hclk/11) 1: By H line
1~0	HVsep1-HVsep0	Multiplexer to select Vsync source: 00: Csync/DE + VsyncSep 01: Hsync + VsyncSep 10: Hsync + VsyncSep XOR Vsync 11: Hsync + Vsync (if SelDE = 1, 00 is chosen, i.e. DE is treated as one kind of Csync)

IntSre (Interrupt Source, 0xD1)		
5	Vint_R	Interrupt is caused by Vsync leading edge 0: Vsync leading edge not happened 1: Vsync leading edge happened
4	Vint_F	Interrupt is caused by Vsync trailing edge 0: Vsync trailing edge not happened 1: Vsync trailing edge happened
3	VfChanged	Interrupt is caused by V frequency change 0: V frequency not changed 1: V frequency changed
2	VpolCha	Interrupt is caused by V polarity change 0: V polarity not changed 1: V polarity changed
1	HfChanged	Interrupt is caused by H frequency change 0: H frequency not changed 1: H frequency changed
0	HpolCha	Interrupt is caused by H polarity change 0: H polarity not changed 1: H polarity changed

SyncStatus (H/V sync signals status, 0xD2)		
6	Falt	Indicate whether Field contains alternating n / n+1 lines 0: Not this format 1: Yes
5	FwHalf	Indicate whether Field contains n+1/2 lines (half line) 0: Not this format 1: Yes
4	Odd_Even	Indicate current field is Odd field or Even field 0: odd field/1st field; with earlier H sync 1: even field/2nd field; with lagged H sync
3	Vpresence	The presence status of Vsync 0: Not present 1: Present
2	Hpresence	The presence status of Hsync/Csync 0: Not present 1: Present

1	Vpolarity	The polarity of Vsync 0: Positive polarity (Pulse width smaller than 1/4 of Vperiod) 1: Negative polarity (Pulse width larger than 3/4 of Vperiod)
0	Hpolarity	The polarity of Hsync 0: Positive polarity (Pulse width smaller than 1/4 of Hperiod) 1: Negative polarity (Pulse width larger than 3/4 of Hperiod)

HperHigh (0xD3)		
7~0	Hperiod15 - Hperiod8	The high nibble of Hperiod (15 - 0)

VHperLow (0xD4)		
7~4	Vperiod7 - Vperiod4	The low nibble of Vperiod (15 - 0)
3~0	Hperiod7 - Hperiod4	The low nibble of Hperiod (15 - 0)

VperHigh (0xD5)		
7~0	Vperiod15 - Vperiod8	The high nibble of Vperiod (15 - 0); it is counted by clock (Hclk/11) or by H line, depending on VcntSel

6.1 PulCnt (H/V output pulse control register, 0xD6)		
7	EnVout	Enable VsyncOut pulse 0: Disabled; VsyncOut is kept low 1: Enabled
6	EnHout	Enable HsyncOut pulse 0: Disabled; HsyncOut is kept low 1: Enabled
5~4	VoutMode1 - VoutMode0	**00 (FreeRun)**: The period of VsyncOut is programmed by 12-bit counter, Vfper. The pulse width is programmed by 4 bit register, Vpw, extended to 6 bits (2, 4, 6, ...28, 30, 32 lines; should be able to cover fly back period). The output waveform is certainly in phase with HsyncOut **01 (Loopth_st)**: The leading edge of VsyncOut will be roughly close to the incoming Vsync, however, snapped to the leading edge of incoming HsyncOut; if the pulse of incoming Vsync is missing, an artificial pulse will be inserted with pulse width defined by VPW. The tailing edge of VsyncOut is also close to the tailing edge of the inputted Vsync but snapped to the leading edge of HsyncOut

		10 (R_aligned): The leading edge of VsyncOut will be shifted ahead or after the leading edge of Vsync based on the programmed value, however, snapped to the leading edge of incoming HsyncOut; if the pulse of incoming Vsync is missing, an artificial pulse will be inserted with pulse width defined by VPW. The pulse width in this mode is also programmable by VPW. **11 (Loopth)**: Completely copy the shape of the incoming Vsync
3~2	HoutMode1 - HoutMode0	**00 (FreeRun)**: The period of HsyncOut is programmed by 10-bit counter, Hfper. The pulse width is programmed by 3-bit register, HPW (0->0.28us, 1->0.59us, 2-> 1.12us, 3->1.40us, 4->1.68us, 5->1.96us, 6->2.23us, 7 ->2.51us) **01 (Loopth_st)**: The HsyncOut will be snapped to the rising/falling edge of incoming Hsync; if the pulse of incoming Hsync is missing, an artificial pulse will be inserted with pulse width defined by HPW. The serration pulses are still kept as the incoming Hsync. The artificial pulse will be inserted after Hperiod/4 + 2 is counted (2 is the tolerance parameter) **10 (R_aligned)**: The leading edge of the output Hsync is aligned with the incoming Hsync. However, the pulse width is defined by HPW. The pulse occurred in the midway of Hsync during serration period is suppressed (Hperiod/8 - 8 is the threshold). An artificial pulse will be inserted while incoming pulse is missing **11 (Loopth)**: Completely copy the shape of the incoming Hsync
1~0	Htolerance1 - Htolerance0	The definition of H frequency/count deviation is programmable: 00: +/- 4 counts 01: +/- 8 counts 10: +/- 16 counts

HVPwth (The Pulse Width of H/V sync output , 0xD7)		
7	EOEnable	The selection of even/odd flag. 0: (default) even/odd flag will be disabled. 1: even/odd flag will be readable and used
6~3	Vpw3 - Vpw0	There are 16 programmable values to set the pulse width of VsyncOut 2*(Vpw + 1) => 2, 4, 6, 30, 32 H lines.

2~0	Hpw2 - Hpw0	The pulse width of Hsync Output: 000: 4(0.28us) 001: 8(0.59us) 010: 16(1.12us) 011: 20(1.40us) 100: 24(1.68us) 101: 28(1.96us) 110: 32(2.23us) 111: 36(2.51us)

PoutPolPos (The polarity of H/V sync output and the position of VsyncOut, 0xD8)		
7~6	VCoastDelay1- VCoastDelay0	When VsyncOut signal is going to scaler as a V sync signal internally, this signal is called VCoast. This control register will generate VCoast Delay by delaying the designated numbers of Hsync at the rising edge of the VsyncOut. The falling edge is almost the same as VsyncOut. 00 : VCoast is the same as VsyncOut 01 : VCoast rising edge is delayed by 1 Hsync from VsyncOut 10 : VCoast rising edge is delayed by 2 Hsync from VsyncOut 11 : VCoast rising edge is delayed by 3 Hsync from VsyncOut Make sure the VsyncOut width is larger the number of Hsync delay, otherwise VCoast can not have a correct falling edge.
5~2	Vshift3 - Vshift0	Vshift(3) = 1 (Leading edge of VsyncOut ahead the incoming Vsync): Vshift2 - Vshift0= 000: Ahead 1 H line 001: Ahead 2 H lines 010: Ahead 3 H lines 011: Ahead 4 H lines 100: Ahead 5 H lines 101: Ahead 6 H lines 110: Ahead 7 H lines 111: Ahead 8 H lines Vshift(3) = 0 (Leading edge of VsyncOut lag the incoming Vsync): Vshift2 - Vshift0= 000: Kept at the same position as incoming Vsync 001: After 1 H line 010: After 2 H lines 011: After 3 H lines 100: After 4 H lines 101: After 5 H lines 110: After 6 H lines 111: After 7 H lines

1	VoutPol	The polarity of VsyncOut 0: Positive polarity (Pulse width smaller than 1/4 of VsyncOut) 1: Negative polarity (Pulse width larger than 3/4 of VsyncOut)
0	HoutPol	The polarity of HsyncOut 0: Positive polarity (Pulse width smaller than 1/4 of HsyncOut) 1: Negative polarity (Pulse width larger than 3/4 of HsyncOut)

HfpHigh (0xD9)		
7~0	Hfperiod9 - Hfperiod2	The high nibble of H free run period (9 - 0)

HvfpLow (0xDA)		
7~6	Vtolerance1 - Vtolerance0	The definition of V frequency/count deviation is programmable: 00: +/- 4 counts 01: +/- 8 counts 10: +/- 16 counts 11: +/- 88 counts
5~2	Vfperiod3 - Vfperiod0	The low nibble of V free run period (11 - 0)
1~0	Hfperiod1 - Hfperiod0	The low nibble of H free run period (9 - 0)

VfpHigh (0xDB)		
7~0	Vfperiod11 -	The high nibble of V free run period (11 - 0)
	Vfperiod4	

7.0 REGISTER DEFINITION FOR TCON (TIMING CONTROL)

The 2-wire serial bus slave address of this chip is 1111100 (bin) (or F8 hex) :

TABLE 24. PANORAMA OF SUB-ADDRESS REGISTER

LOW NIBBLE OF SUBADDRESS																	
	Addr (hex)	X0 H	X1 H	X2 H	X3 H	X4 H	X5 H	X6 H	X7 H	X8 H	X9 H	XA H	XB H	XC H	XD H	XE H	XF H
HIGHNIBBLE	0XH	reserved	TC_MAJOR1	TC_MAJOR2													
	1XH	GPO0 Programming Registers										LP Programming Registers					
	2XH	GPO1 Programming Registers CLKV Programming Registers															
	3XH	STH Programming			POL Programming					CLKH Programming Registers							
	4XH	STV Programming and CLKV_VSTART															
	5XH	GPO2 Programming Registers									RESERVED						
	6XFXH	RESERVED															

TC_MAJORI (TCON MAJOR control register 1, 02H)			**Default**
7	LP_PHASE	The phase selection of the edges of LP pulse signal with respect to the internal pixel clock. 0: (default) Aligned with the rising edge of CLKH. 1: Aligned with the falling edge of CLKH. NOTE: Internal pixel clock, CLKH, will send to Pin 63 which can be inverted with programmable delay. Please refer to PHCLK_INV and PHCLK_OP in RegisterOUTCTR0 or 03hex.	0
6	TI_MODE	STV start position (This bit also defines the CLKV start position) 0: (default) Normal start. 1: Late start.	0
5	POL_MODE	The toggle duration of POL (polarity output signal) pin 0: (default) toggle per H line. 1: toggle per 2H lines	0

4	CLKH_OFF	The CLKH signal can be turned off during the non-active display period. 0: (default) CLKH output signal is always available. 1: CLKH signal will be turned off during the non-active display period. The duration is defined by the TC_CLKH_VSTART, TC_CLKH_VACTIVE, TC_CLKH_HSTART, and TC_CLKH_HACTIVE registers.	0

TC_MAJORI (TCON MAJOR control register 1, 02H)			**Default**
3	RGB_BUS_SKEW	Data bus group delay for EMI reduction. 0: (default) The data bus of RGB signals are distributed as 0.0/1.0/2.0ns. 1: The data bus of RGB signals are distributed as 0.0/2.0/4.0ns.	0
2	DIRECTION_SCMD	The driver IC R/L direction control. 0: (default) The output of STV1 and STH1 pins are available. And RLSC is high. (Note: The output of STV3 and STH8 pins have no signals.) 1: The output of STV3 and STH8 pins are available. And RLSC is low. (Note: The output of STV1 and STH1 pins have no signals.)	0
1	INVERSE_HMS	The inversion of HMSO and HMSE signals. 0: (default) No inversion. 1: The HMSO and HMSE signals will be inversed	0
0	ENABLE_HMS	The operation of HMSO and HMSE signals. 0: The HMSO and HMSE signals will be kept at high or low (In a word, HMSO=HMSE=INVERSE_HMS). 1: (default) The operation of HMSO and HMSE is enabled.(Note: HMSO and HMSE will be calculated separately)	1

TC_MAJOR2 (TCON MAJOR control register 2, 03H)			**Default**
7	INVERSE_CLKV	The inversion of CLKV clock. 0: (default) No inversion. 1: Inversed CLKV.	0
6	TCON_8BIT	TCON can be configured for 8-bit or 6-bit (for each RGB) TFT-LCD panel 0: (default) TCON is configured for 8-bit (for each RGB) panel. 1: TCON is configured for 6-bit (for each RGB) panel	0
5	SINGLE_HMS	This register defines the operation of HMS is based on two single port (24/18 bits) or one dual port (48/36 bits) 0 : EVEN/ODD is calculated separately 1 : EVEN/ODD is calculated together	

REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE	R/W	Description
Major feature Control Register TC_MAJOR1[7:0]	01	00	W	Major programming features of the timing controller 1
Major feature Control Register TC_MAJOR2[7:0]	02	00	W	Major programming features of the timing controller 2
Reserved	03-0F	00	W	
GPO0 Horizontal Start TC_GPO0_HSTART[10:0]	11, 10	01,28	W	Define the GPO0 horizontal start counter value.
GPO0 Horizontal Active TC_GPO0_HACTIVE[10:0]	13, 12	02,94	W	Define the GPO0 horizontal active duration counter value.
GPO0 Vertical Start TC_GPO0_VSTART[10:0]	15, 14	00,23	W	Define the GPO0 vertical start counter value.
GPO0 Vertical End TC_GPO0_VEND[10:0]	17, 16	03,00	W	Define the GPO0 vertical end duration counter value.
GPO0 Control Register TC_GPO0_CONTROL[7:0]	18	00	W	Define the GPO0 control value. TC_GPO0_CONTROL[1:0] defines = 00 : no logical operation, = 01 : inverted, = 10 : toggled on rising edge, = 11 : toggled then inverted.
Reserved	19	00	W	
LP Horizontal Start TC_LP_HSTART[10:0]	1B, 1A	01,28	W	Define the LP signal horizontal start counter value.
LP Horizontal Active TC_LP_HACTIVE[6:0]	1C	04,00	W	Define the LP signal horizontal active duration counter value.
Reserved	1D	00	W	
LP Vertical End TC_LP_VEND[10:0]	1F, 1E	00,23	W	Define the LP signal vertical end counter value.
GPO1 Horizontal Start TC_GPO1_HSTART[10:0]	21, 20	01,28	W	Define the GPO1 horizontal start counter value.
GPO1 Horizontal Active TC_GPO1_HACTIVE[10:0]	23, 22	02,94	W	Define the GPO1 horizontal active duration counter value.
GPO1 Vertical Start TC_GPO1_VSTART[10:0]	25, 24	00,23	W	Define the GPO1 vertical start counter value
GPO1 Vertical End TC_GPO1_VEND[10:0]	27, 26	03,00	W	Define the GPO1 vertical end duration counter value.

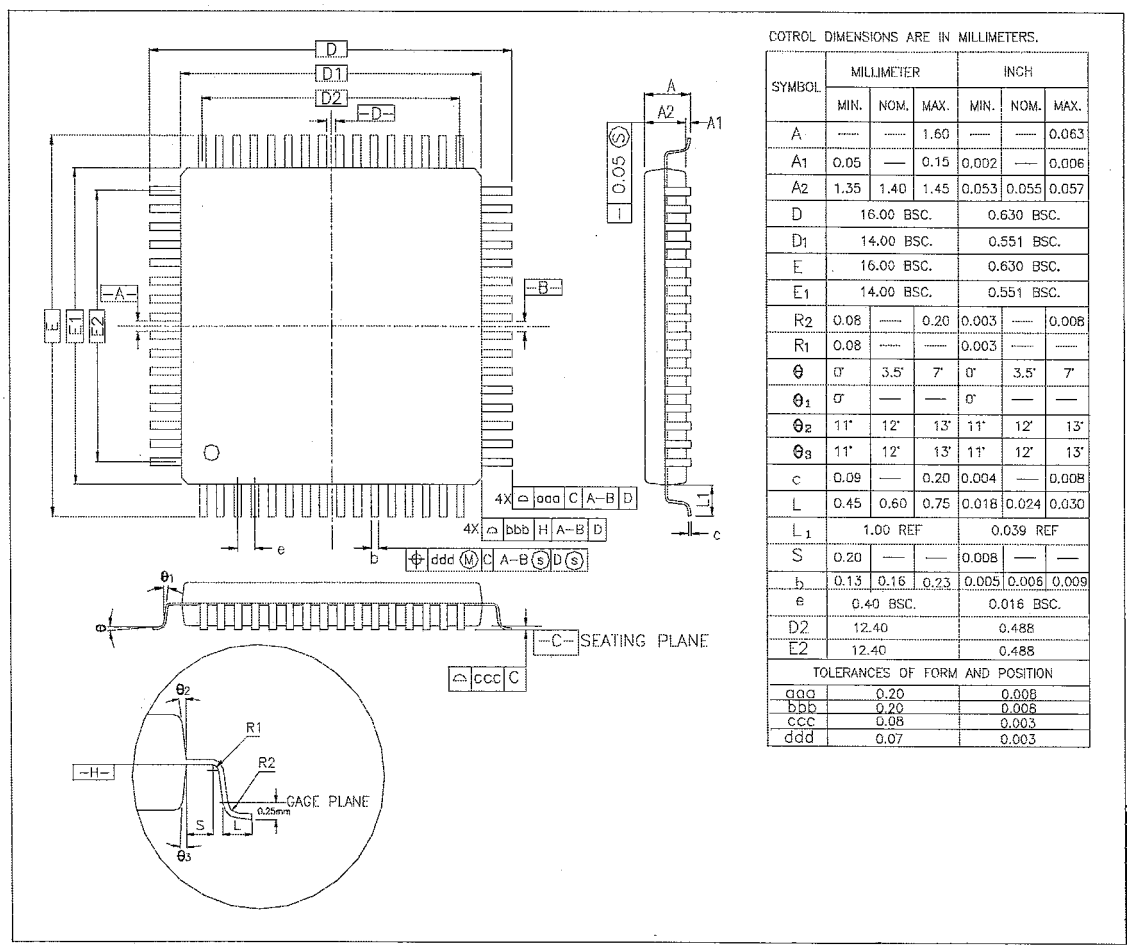
GPO1 Control Register TC_GPO1_CONTROL[7:0]	28	00	W	Define the GPO1 control value TC_GPO1_CONTROL[1:0] = 00 : no logical operation, = 01 : inverted, = 10 : toggled on rising edge, = 11 : toggled then inverted. The value will then perform logical operation (with the signal from GPO0) defined by TC_GPO1_CONTROL[3:2] defines = 00: no logical operation, = 01: AND with TC_GPO0, = 10: OR with TC_GPO0, = 11: select TC_GPO0 or TC_GPO1 alternately on the rising edge of HS or VS which is selected by TC_GPO1_CONTROL[4] = 0 : toggle on HS = 1: toggle on VS.
Reserved	29	00	W	
CLKV Horizontal Start TC_CLKV_HSTART[10:0]	2B, 2A	01,28	W	Define the CLKV signal horizontal start counter value.
CLKV Horizontal Active TC_CLKV_HACTIVE[9:0]	2D, 2C	04,00	W	Define the CLKV signal horizontal active duration counter value.
CLKV Vertical End TC_CLKV_VEND[10:0]	2F, 2E	00,23	W	Define the CLKV signal vertical end counter value. NOTE: The vertical start of the CLKV signal is defined by the position of STV pulse (so called Ti_mode). Also the V start value of CLKV is defined at TC_STVCLKV_VSTRAT[3:0].
STH Horizontal Start TC_STH_HSTART[10:0]	31, 30	01,28	W	Define the STH signal horizontal start counter value. NOTE: The active duration of STH pulse is always one-pixel width.
STH Vertical End TC_STH_VEND[10:0]	33, 32	00,23	W	Define the STH signal vertical end counter value

POL Horizontal Start TC_POL_HSTART[10:0]	35, 34	01,28	W	Define the POL signal horizontal start counter value. NOTE: The POL signal can be toggled every H line or every 2H lines. Please refer to the bit POL_MODE in TCON_MAJOR register
POL Vertical End TC_POL_VEND[10:0]	37, 36	00,23	W	Define the POL signal vertical end counter value.
CLKH Horizontal Start TC_CLKH_HSTART[10:0]	39, 38	01,28	W	Define the CLKH horizontal start counter value. NOTE: To save power consumption, CLKH can be deactivated during the non-active display period. Please refer to CLKH_OFF in TCON_MAJOR register.
CLKH Horizontal End TC_CLKH_HEND[10:0]	3B, 3A	04,00	W	Define the CLKH horizontal end duration counter value.
CLKH Vertical Start TC_CLKH_VSTART[10:0]	3D, 3C	00,23	W	Define the CLKH vertical start counter value.
CLKH Vertical End TC_CLKH_VEND[10:0]	3F, 3E	03,00	W	Define the CLKH vertical end duration counter value.
STV Horizontal Start TC_STV_HSTART[10:0]	41, 40	01,28	W	Define the STV signal horizontal start counter value.
STV Horizontal Active TC_STV_HACTIVE[11:0]	43, 42	00,14	W	Define the STV signal horizontal active counter value
STV and CLKV Vertical Start TC_STVCLKV_VSTRAT[7:0]	44	00	W	Define the vertical start counter value of STV and CLKV. TC_STVCLKV_VSTRAT[3:0] is for the V start value of CLKV and TC_STVCLKV_VSTRAT[7:4] is for the V start value of STV
TC_LNUM_AHEAD_DE[10:0]	46,45	00,01	W	Define the number of lines that is ahead DENA; the Vertical value is calculated from this point
TC_STH_WIDTH[7:0]	47	00	W	Define the width of STH pulse
Reserved	48-4F	00	W	
GPO2 Horizontal Start TC_GPO2_HSTART[10:0]	51, 50	01,28	W	Define the GPO2 horizontal start counter value.
GPO2 Horizontal Active TC_GPO2_HACTIVE[10:0]	53, 52	02,94	W	Define the GPO2 horizontal active duration counter value

GPO2 Vertical Start TC_GPO2_VSTART[10:0]	55, 54	00,23	W	Define the GPO2 vertical start counter value.
GPO2 Vertical End TC_GPO2_VEND[10:0]	57, 56	03,00	W	Define the GPO2 vertical end duration counter value
GPO2 Control Register TC_GPO2_CONTROL[7:0]	58	00	W	Define the GPO2 control value. TC_GPO2_CONTROL[1:0] = 00 : no logical operation, = 01 : inverted, = 10 : toggled on rising edge, = 11 : toggled then inverted. The value will then perform logical operation (with the signal from GPO1) defined by TC_GPO2_CONTROL[3:2] defines = 00: no logical operation, = 01: AND with TC_GPO1, = 10: OR with TC_GPO1, = 11: select TC_GPO1 or TC_GPO2 alternately on the rising edge of HS or VS which is selected by TC_GPO2_CONTROL[4] = 0 : toggle on HS = 1: toggle on VS
Reserved		00	W	

8.0 PACKAGE OUTLINE

8.1 128l LQFP

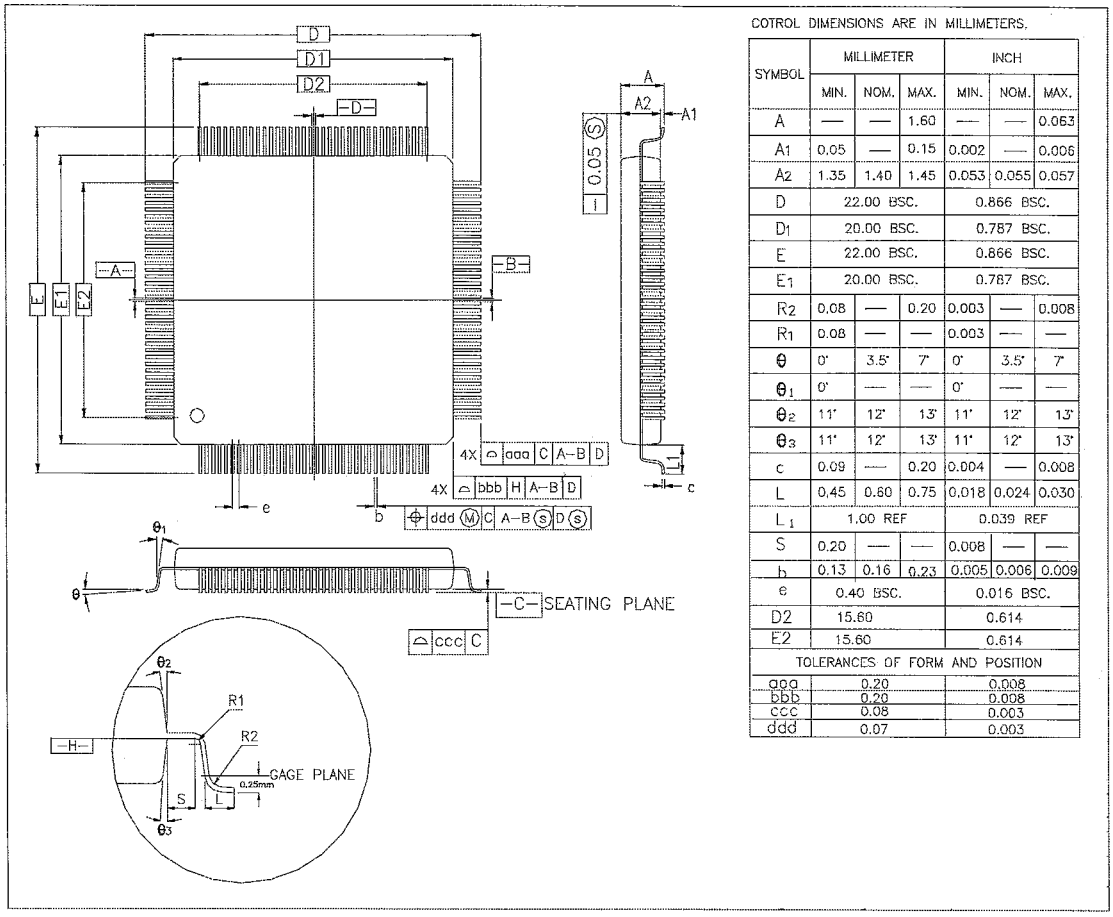


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.60	-----	-----	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	-----	0.20	0.003	-----	0.008
R1	0.08	-----	-----	0.003	-----	-----
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		

TOLERANCES OF FORM AND POSITION		
aaa	0.20	0.008
bbb	0.20	0.008
ccc	0.08	0.003
ddd	0.07	0.003

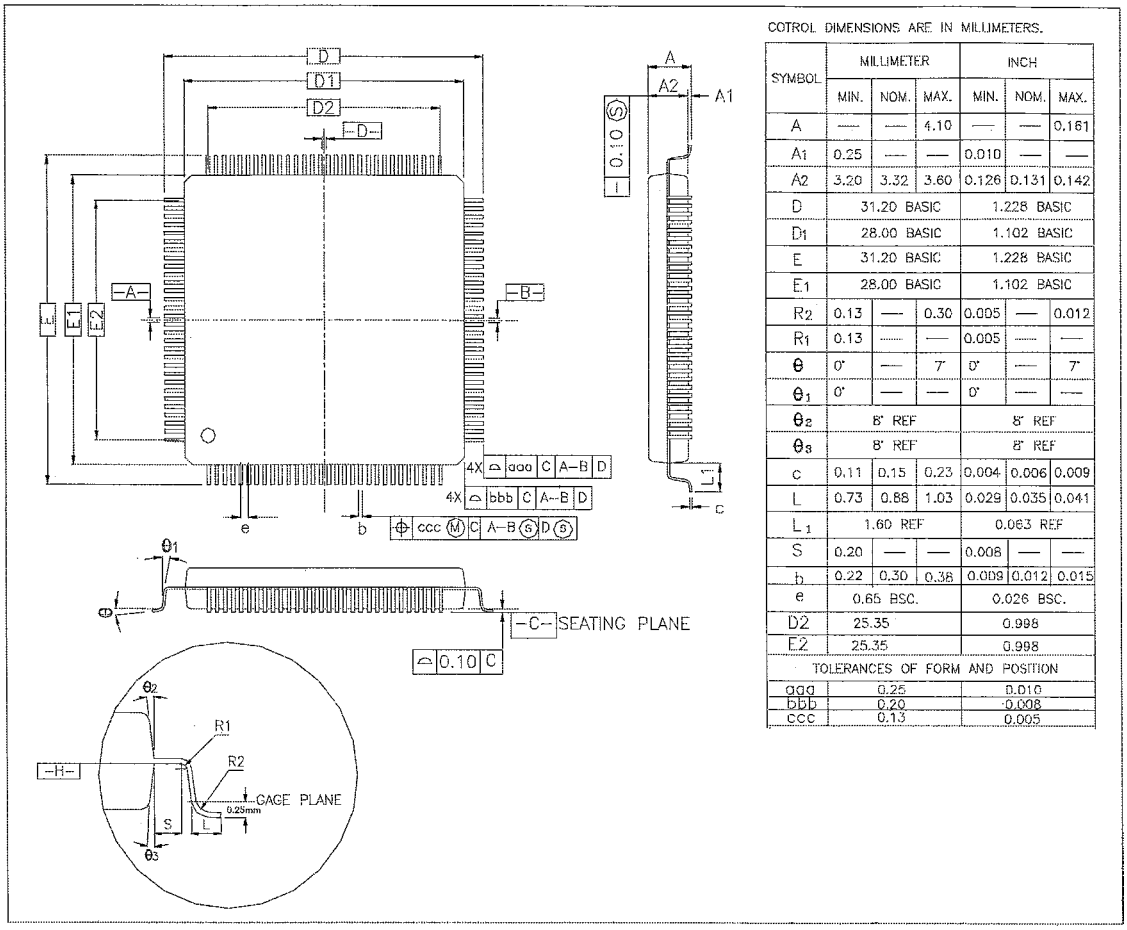
8.2 160L LQFP



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	22.00 BSC.			0.866 BSC.		
E1	20.00 BSC.			0.787 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	15.60			0.614		
E2	15.60			0.614		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

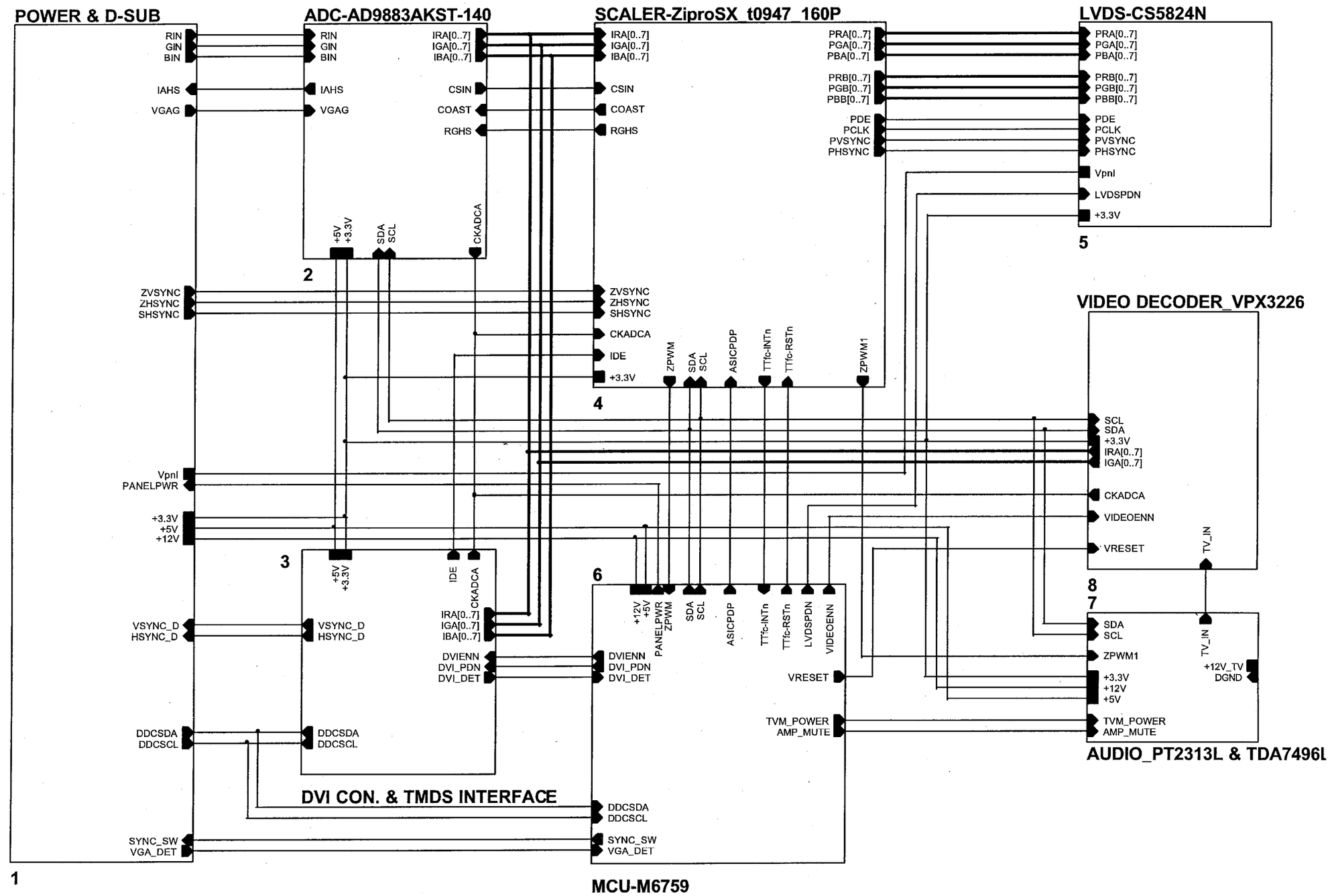
8.3 160 QFP



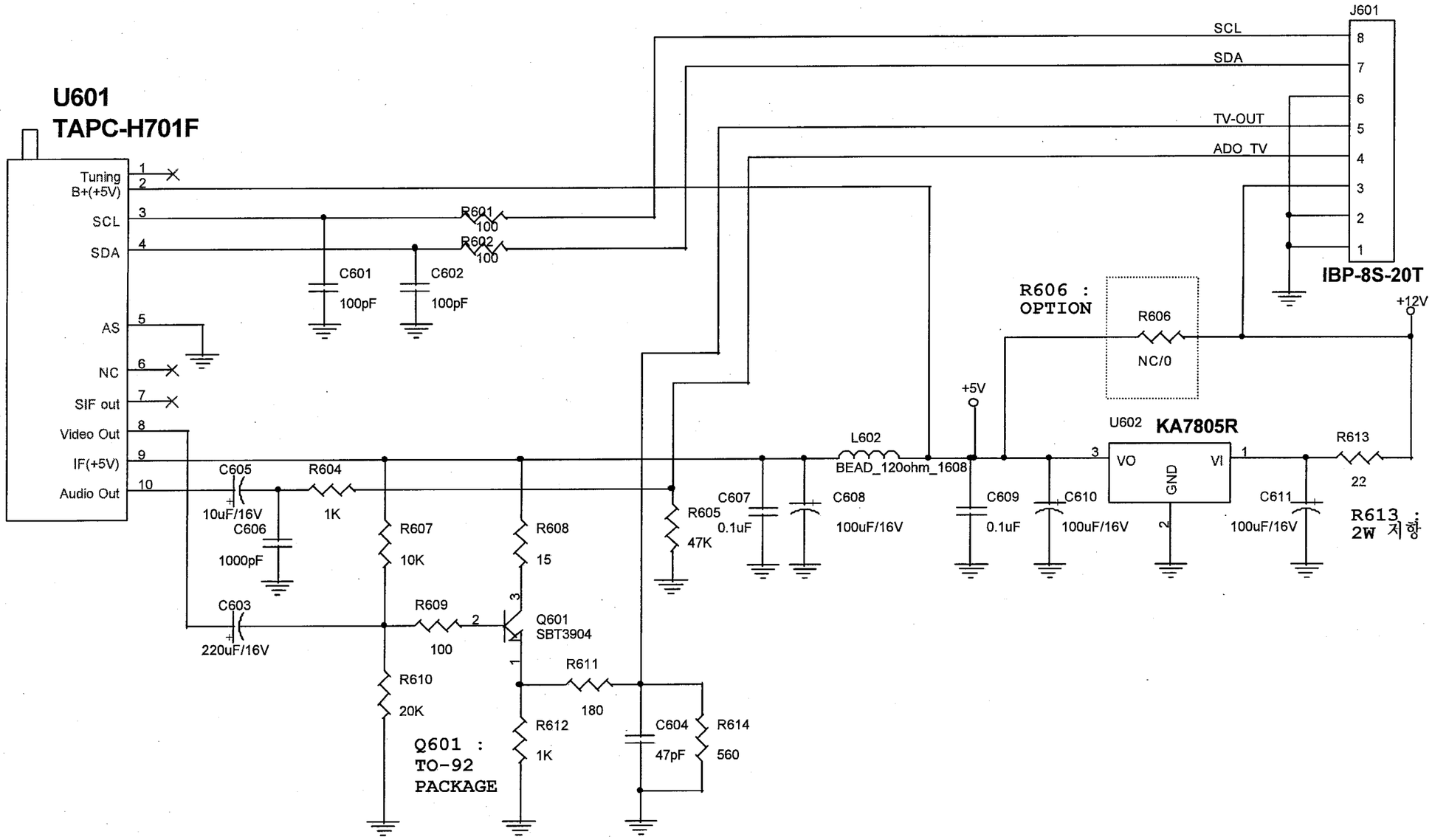
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A1	0.25	—	—	0.010	—	—
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E1	28.00 BASIC			1.102 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	8° REF			8° REF		
θ3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.65 BSC.			0.026 BSC.		
D2	25.35			0.998		
E2	25.35			0.998		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.13			0.005		

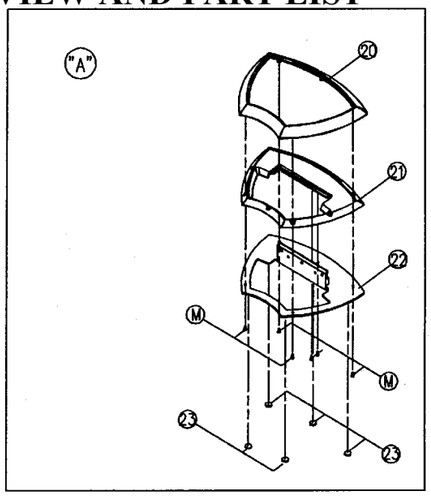
BLOCK DIAGRAM

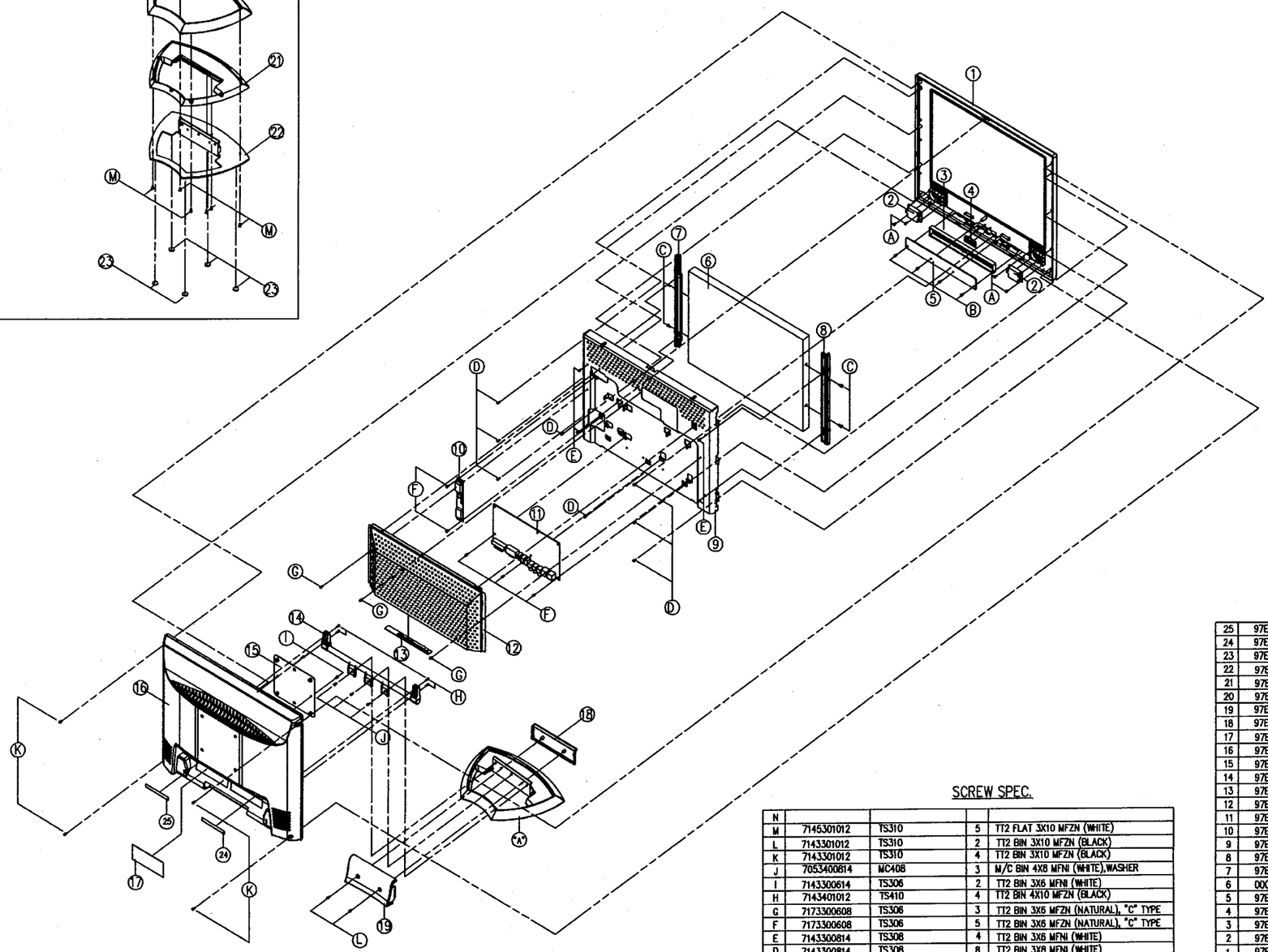


TV TUNER


U601
TAPC-H701F
Tuning B+(+5V)
SCL
SDA
AS
NC
SIF out
Video Out
IF(+5V)
Audio Out
R601 100
R602 100
C601 100pF
C602 100pF
C605 10uF/16V
R604 1K
C606 1000pF
R607 10K
R608 15
C603 220uF/16V
R609 100
Q601 SBT3904
R610 20K
R611 180
R612 1K
C604 47pF
R614 560
Q601 : TO-92 PACKAGE
R605 47K
C607 0.1uF
C608 100uF/16V
L602 BEAD_120ohm_1608
C609 0.1uF
C610 100uF/16V
U602 KA7805R
VO
GND
VI
C611 100uF/16V
R613 22
R613 : 2W 저항
R606 : OPTION
R606 NC/0
+5V
+12V
J601
SCL
SDA
TV-OUT
ADO_TV
IBP-8S-20T

EXPLODED VIEW AND PART LIST





SCREW SPEC.

NO.	PART NO.	PART NAME	Q'TY	SPEC.
N				
M	7145301012	TS310	5	TT2 FLAT 3X10 MFZN (WHITE)
L	7143301012	TS310	2	TT2 BIN 3X10 MFZN (BLACK)
K	7143301012	TS310	4	TT2 BIN 3X10 MFZN (BLACK)
J	7053400814	MC408	3	M/C BIN 4X8 MFNI (WHITE),WASHER
I	7143300614	TS306	2	TT2 BIN 3X6 MFNI (WHITE)
H	7143401012	TS410	4	TT2 BIN 4X10 MFZN (BLACK)
G	7173300608	TS306	3	TT2 BIN 3X6 MFZN (NATURAL), "C" TYPE
F	7173300608	TS306	5	TT2 BIN 3X6 MFZN (NATURAL), "C" TYPE
E	7143300814	TS308	4	TT2 BIN 3X8 MFNI (WHITE)
D	7143300814	TS308	8	TT2 BIN 3X8 MFNI (WHITE)
C	7003300814	MC308	4	M/C BIN 3X8 MFNI (WHITE)
B	7143300814	TS308	4	TT2 BIN 3X8 MFNI (WHITE)
A	7143300814	TS308	4	TT2 BIN 3X8 MFNI (WHITE)

NO.	PART NO.	PART NAME	Q'TY	MATERIAL	SPEC.
25	97E1901200	LABEL IO A	1	PE FILM	
24	97E1901300	LABEL IO B	1	PE FILM	
23	97E1800300	RUBBER FOOT	5	NBR	
22	97E7401300	BKT STAND	1	SPCC T=3.0	
21	97E43008XX	STAND BOTTOM	1	ABS(HF380)	
20	97E43009XX	STAND DECO	1	ABS(HF380)	
19	97E43011XX	STAND BACK	1	ABS(HF380)	
18	97E43010XX	STAND FRONT	1	ABS(HF380)	
17	97E19010XX	LABEL RATING - A	1	PET SILVER T=0.1	
16	97E01008XX	COVER BACK	1	ABS(HF380)	
15	97E7402000	BKT VESA	1	EGI T=1.0	
14	97EA302400	HINGE LCD AS	1	AL (DIE CASTING)	
13	97E0600110	PLATE IO	1	PVC 0.5T	
12	97E7401200	BKT SHIELD	1	EGI T=0.5	
11	97EA302301	PCB AD AS	1		
10	97EA302100	PCB INVERTER AS	1		
9	97E7401101	BKT LCD	1	EGI T=0.8	
8	97E1101200	HOLDER LCD R	1	ABS(HF380)	
7	97E1101100	HOLDER LCD L	1	ABS(HF380)	
6	0000000000	LCD MODULE	1		
5	97EA302010	PCB OSD AS	1		
4	97E46003XX	CAP LED	1	ACRYL	
3	97E10006XX	KEYTOP OSD	1	ABS(HF380)	
2	97EA302500	SPEAKER AS	2		
1	97E01007XX	COVER FRONT	1	ABS(HF380)	