# CGVI8

31-aug-2004.
Embedded software version 5.

## 1. Features

The device is designed for timing in control systems of accelerators. The device generates 8 output pulses delayed concerning to input start pulse.

The device includes:

- 8 channels delayed pulse generator;
- 8-channel output register with galvanically isolated outputs;
- 8-channel input register with galvanically isolated inputs;
- CANbus interface for interaction with control computer;
- micro-controller.

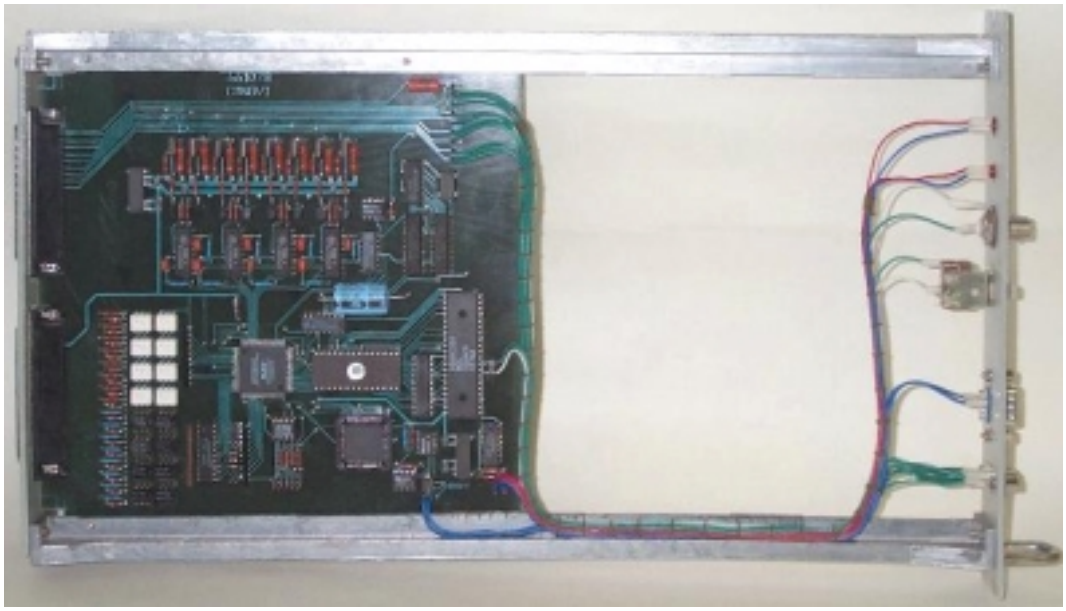


Photo of device

The device can be interpreted as 8 independent delayed pulse generators with common start inputs. The start input of the device is galvanically isolated and all outputs have common “ground” connected with power supply. All inputs may be disabled by bit field mask. It gives additional opportunities for an user. A time quantum of device may be changed by user. The device is provided by a pair registers with galvanic isolation. These registers are very useful in different automation systems.

The pulse generators are implemented in PLD. As a result, a system traffic and software tricks cannot affect on stability and jitter of output pulses. The device is intended to be embedded in “WISHNYA” racks. The device requires for proper operation the only power supply with voltage +5V (±5%).

## 2. Specifications:

1. Resolution of the pulse generator - 16 bits.
2. Output channels – 8.
3. Input resistance – 75 Ohm.
4. Output voltage +12÷15 V.
5. Output pulse duration - 1-5 mcSec.
6. Terminator resistance 75 Ohm.
7. Time quantum (discreteness) - 100 nS or more (programmable).
8. Jitter – 10 nS.
9. Delay for code 0000 – 250 nS.
10. Voltage of start pulse 5-24 V.
11. Duration of start pulse – 50 nS.
12. Accuracy of internal timing - 0.1%.
13. Channels of output register- 8.
14. Maximal voltage for output register- 50V.
15. Maximal current for output register- 32 ma.
16. Channels of output register- 8.
17. Voltage for input register- 2.5-6.0V.
18. Input resistance for input register- 510 Ohm.
19. Maximum working insulation voltage for input/output registers - 1500 B.
20. CANbus transceiver is galvanically isolated from network and it is in compliance with ISO 11898-24V (chip PCA82C251).
21. Hardware implementation allows using both standard and extended CANbus frames. Software implementation is based on standard frames (short identifier).
22. Baud rates- 1000, 500, 250, 125 Kbaud (may be chosen by jumpers).
23. Voltage of power supply- +5V, ±5%.
24. Power supply current- <0.5A (typical value- 0.35A).

## 3. External connections

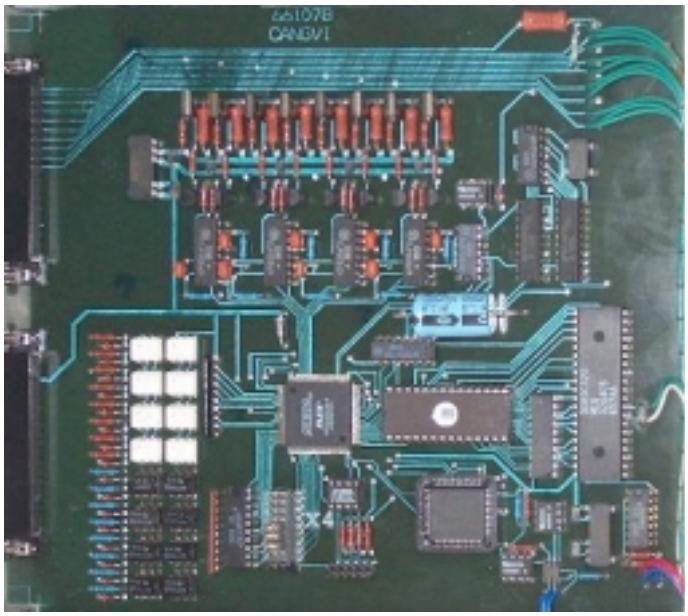
The device is implemented as module in “WISHNYA” standard, width is 40 mm. A front panel of the device contains a network connector (DB-9M), auxiliary connector (DB-9F) for checking output pulses, SR50-73F for connecting with start pulse source, RESET button and two LEDs. One LED is blinking during processing CANbus message. The second LED is on during delay generation process. Connection with external channels of control and measurements carry out by DRB-37M connectors on back panel. Analog output and inputs of device are connected with pins of X1 connector. Outputs and inputs of registers are connected with X2 connector.

A connection of inputs/outputs with controlled devices should be done by a connectors (DB27) on a rare panel. X1 connector provides delayed pulse outputs and start input. X2 connector provides inputs and outputs of registers.

## 3.1. Jumpers

The device has a set of jumpers (they are labeled on the photo as X4). 6 jumpers define number (address) of device in network (this number is used to compose identifier of messages) and 2 jumpers define baud rate.

Jumpers location is shown below on board photo.




Jumpers location on board.

Destination of jumpers in X4 group.

| Designation | Location | Destination |
|---|---|---|
| X4-7 | Upper | N5- included in device number (most significant bit) |
| X4-6 | … | N4- included in device number |
| X4-5 | … | N3- included in device number |
| X4-4 | … | N2- included in device number |
| X4-3 | … | N1- included in device number |
| X4-2 | … | N0- included in device number (least significant bit) |
| X4-1 | … | BR1- defines baud rate |
| X4-0 | Lower | BR0- defines baud rate |

Jumpers N5…N0 defines logical number (address) of device which is used to compose message identifier for CANbus network (for more detail see PROTOCOL part of this description). An installed jumper should be interpreted as logical 0 and absence of jumper should be interpreted as logical 1.

Baud rate defining.

| BR1 | BR0 | Baud rate |
|---|---|---|
| Connected | Connected | 1000 Kbit/sec |
| Connected | Disconnected | 500 Kbit/sec |
| Disconnected | Connected | 250 Kbit/sec |
| Disconnected | Disconnected | 125 Kbit/sec |

**NOTES:**

1. CANbus is bus with multiple access and incorrect baud rate setting may affect on transfer messages of other devices in addition to impossibility of access to this device.

In network may exist concurrently devices with identical numbers (addresses). Formally it is permissibly, but actually it do cause a lot of problem. Connecting to network devices with identical numbers is strictly not recommended.

## 3.2 Front panel.

A front panel includes:


**Line** LED
**Run** LED
**Reset** button
**Start** connector
**CANbus** connector
**Control** connector

**Line** LED is blinking during processing CANbus messages by onboard processor.

**Run** LED is turned ON by start pulse and turned OFF by a pulse generation process (65536 time quantum). So, blinking LED means process og pulse generation.

After power-on the device blinks by all LEDs a few times.

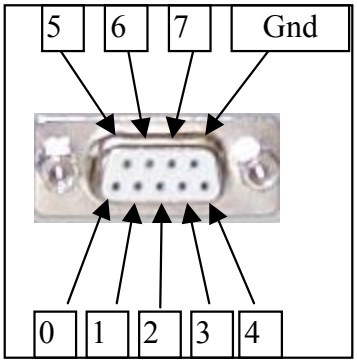
**Reset** button is intended for hardware reset. It isn't intended for daily using.

Разъем **Start** предназначен для подачи блоку стартового импульса.

**CANbus** connector (DB-9M) is intended for connection to media. Pin designations follows below in table.

| | | |
|---|---|---|
| 2 | CAN-L | One wire in pair |
| 3 | GND | Shield of cable |
| 7 | CAN-H | One wire in pair |

Shielded twisted pair is used as media. According to the ISO 11898-2 it should has a nominal impedance 120 Ohm. Line termination has to be provided through termination resistors of 120 Ohm located at both ends of the line.




**Control** connector is intended for checking of output pulses (by oscilloscope, for example). It may be used for connection with controlled device also. There is used DB9F connector.

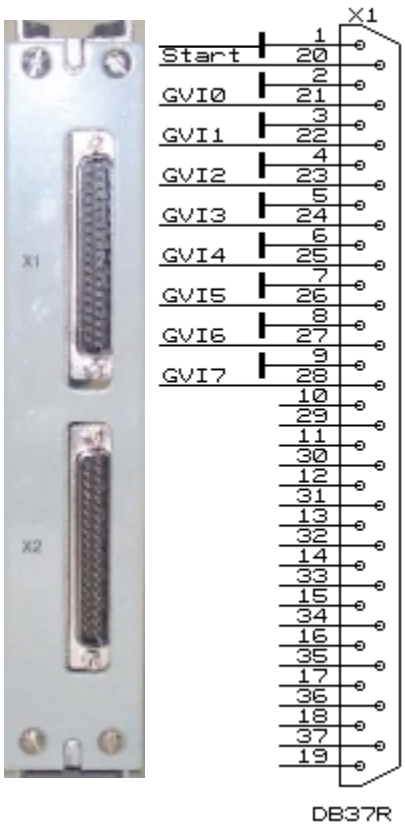
A table below shows pin-out of the connector.

| Pin of DB-9F connector | Destination |
|---|---|
| 1 | Channel 0 output |
| 2 | Channel 1 output |
| 3 | Channel 2 output |
| 4 | Channel 3 output |
| 5 | Channel 4 output |
| 6 | Channel 5 output |
| 7 | Channel 6 output |
| 8 | Channel 7 output |
| 9 | Common wire («ground») |

## 3.3 Back panel.

A two connectors (DRB-37M) are placed on the back panel. Connection external devices with CGVI8 should be done through these connectors. X1 connector contains pulse outputs and X2 connector includes outputs and inputs of registers and power supply pins.

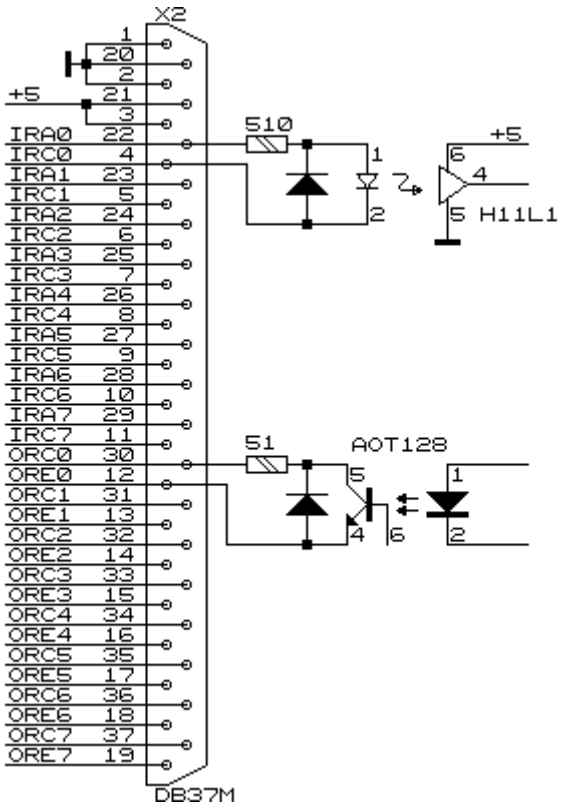
### 3.3.1 X1 connector.




X1 connector provides outputs of delayed pulses and start pulse input. All outputs have common wire connected with “ground” of the device. “Ground” wire of start pulse input are not connected with “ground” of the device. The start pulse input is galvanically isolated from device “ground”.

If a start pulse source has floating output an user must connect “ground” wire (pin 1) of the input with “ground” of CGVI8. If a start pulse source is connected with “ground” there is nothing to do.

### 3.3.2 X2 connector.




X2 connector provides pins of input and output registers. Powering of the device should be done through pins of X2. The device requires the only external power supply with voltage +5V (±5%). There is shown a location of signals on the connectors pins. A fragment of circuitry is included to show an implementation of input and output registers. Both registers are designed with galvanic isolation which is provided by optocouplers.

Design of input register is based on a chip H11L1. It is intended for detection external voltage or current. Input voltage range is from 3V to 12V. Input current range is from 4mA to 20mA. Unconnected input (no current in LED) is interpreted as logical 0.

Output register design is based on transistor optocoupler and it is able to provide output current up to 32mA. Output voltage may be up to 30V.

## 4. Basics of operations for CGVI-8

As was mentioned above the device includes the following components:

- a multi-channel delayed pulse generator;
- an input register with optical isolation of inputs;
- an output register with optical isolation;
- CANbus interface;
- a micro-controller for integration all parts of the device and interaction with control computer.

Logically, input and output registers are not connected with pulse generator and they are controlled by separate CANbus messages. After power-up the micro-controller writes to pulse generator channels codes corresponding zero delay, writes zero into output register, mask register, base register and sends to host a power-up message. Writing zero into mask register leads to disabling of output pulses. Output pulse delay registers are separate for each channel, but mask register and base register are common for all channels.

After an initialization sequence the device passes to a work state. After receiving a start pulse it begins to form a delayed output pulses. The process is going on by the following way. The start pulse is clocked by internal 100 MHz generator to provide a jitter no more than 10 nS. Then, synchronized start pulse switch a prescaler counter and a main counter from IDLE state to PROCESS state. The prescaler counter is intended for changing a time quantum and, accordingly, a time base of device. Each time quantum a value of main counter is incremented. When a main counter value coincides with code in some delay register a corresponding output generates an

output pulse. Any start pulses are ignored up to completion of counting main counter (work cycle length).

| Prescaler code | Time quantum | Work cycle length |
|---|---|---|
| 0 | 100 nS | 6.5536 mSec |
| 1 | 200 nS | 13.1072 mSec |
| 2 | 400 nS | 26.2144 mSec |
| 3 | 800 nS | 52.4288 mSec |
| 4 | 1.6 mcSec | 104.8576 mSec |
| 5 | 3.2 mcSec | 209.7152 mSec |
| 6 | 6.4 mcSec | 419.4304 mSec |
| 7 | 12.8 mcSec | 838.8608 mSec |
| 8 | 25.6 mcSec | 1.678 Sec |
| 9 | 51.2 mcSec | 3.355 Sec |
| 10 | 102 mcSec | 6.711 Sec |
| 11 | 205 mcSec | 13.42 Sec |
| 12 | 410 mcSec | 26.84 Sec |
| 13 | 819 mcSec | 53.68 Sec |
| 14 | 1.64 mSec | 107.4 Sec |
| 15 | 3.28 mSec | 214.7 Sec |

A start pulse may be generated by computer command.

There is a mask register. The mask register allows disabling output pulses on selected outputs. A least significant bit disables (enables) output 0 and most significant bit disables (enables) output 0, correspondingly. When corresponding bit is 0 the output is disabled, when corresponding bit is 1 the output is enabled. A power-up sequence clears the mask register to prevent initiating controlled devices before defining correct delays.

There is a limit register (1 byte). When the high byte of main counter reaches a limit register value the device is switched from PROCESS state to IDLE state. A power-up sequence clears the limit register.

| Limit register value | Work cycle length (quants) |
|---|---|
| 0 | 65535 |
| 1 | 256 |
| 2 | 512 |
| … | … |
| 255 | 65280 |

For correct application of the device an user should understand how the value, stability, uncertainty of delay depend on. The value of delay is formed from:

$$T = Tq*Code + Td + Ta + Tj$$

Here:

T – value of delay;
Tq – time quantum;
Code – code in delay register;
Td – digital component of input circuitry delay;
Ta – analog component of input circuitry delay;
Tj – time of jitter.

In this equation the first component is ideal and absolutely accurate. Td (digital component of additional delay) is constant and it equals 100 nSec. This component don’t have an influence on

delay stability. Ta (analog component of additional delay) is defined by input circuitry (opto-coupler, gates) delay. It's value (approximately 100 nSec) depends on temperature, power supply voltage and it has a bit different value in different modules. Tj (jitter time) is defined by circuitry which synchronized input start pulse to internal generator. The value of this delay is 0÷10 nSec.

## 5. A command set for CGVI-8

Identifier bits distribution

| Identifier bits | ID10…ID08 | ID07...ID02 | ID01…ID00 |
|---|---|---|---|
| Bit field | Field 1 | Field 2 | Field 3 |
| Destination | Priority | Address | Reserve |

Comments to bit distribution:

Field 1 – priority field (type field):
Code 5 – a broadcast message (field 2 is ignored).
Code 6 – ordinary (address) message.
Code 7 – response (reply for type 6 message).
Code 0 is forbidden, other combination is not used (they are reserved for future extensions).

Field 2 – a physical address field. It defined address device (this address is defined by jumpers on-board).

Field 3: User should set zero in this field. The device can send messages with different values in this field.

Any device on receiving address message interprets an information by its content. If received message requires a reply, the device sends required information by message with code 6 (response type message). A broadcast messages should be received by all devices simultaneously and required actions should be done in all devices.

An interpretation of data fields:
On receiving message a device interprets data in following way: a first byte (byte 0) is descriptor of message, the other bytes are an additional information.

There is a list of message descriptors (codes are hexadecimal).
00 - 07 – write a delay code to CGVI-8 channel 0 - 7
10 - 17 – request delay code from CGVI-8 channel 0 – 7

F0 – write of mode (configuration of the device)
F1 – write of limit register
F7 – start from computer
F8 - request for data from input and output registers
F9 - write to output register
FE – device status request
FF - device attributes request

On receiving a request for data message the device sends to host a response message. In the response message the first data byte contains the same value as the first data byte in request message. On receiving a write data message the device don't send any message in reply.

**Detail description of messages for CGVI8**
**(all codes are hexadecimal)**

**00 - 07** – (write to delay register of CGVI8 channel 0-7), the following bytes are data bytes.
Example:

| | | |
|---|---|---|
| 04 | 12 | 11 |
| 4th channel | Byte 0 | Byte 1 |

This message places into 4-th CGVI channel value 2828 (decimal). If time quantum equals 100 nSec then this value defines delay as 282.8 mcSec.
Byte 1 is the most significant byte and byte 1 is the least significant byte.

**10 - 17** – (request code from delay register of CGVI8 channel 0-7). The following bytes will be ignored. In reply the device sends a message with the same code but with data from delay register (bytes 0, 1).

**F0** – write of mode (configuration of the device).

| | | |
|---|---|---|
| F0 | Mask | Prescaler |

Mask – a bit-field mask register. Bit b0 controls of channel 0. If bit is cleared then controlled channel is disabled.

Prescaler- this register controls of time quantum there is used only 4 bits. Code 0 defines time quantum as 100 nSec and so on.

**F1** – write limit register.

| | |
|---|---|
| F1 | Limit |

This command is valid only if hardware version is not 1 and software version is above 4.

**F7** – start from computer, there is not parameters.

**F8** - request date from registers. This message has not additional information. In reply a device sends a message with output register byte and input register byte.

| | | |
|---|---|---|
| F8 | Output Register Data | Input Register Data |

**F9** - write data to output register.
Byte 1 contains information to be written into output register. The device don't respond on this message.

| | |
|---|---|
| F9 | Output Register Data |

**FE** - request device status. It hasn't any parameters. In reply a device sends the following message:

| | | | | |
|---|---|---|---|---|
| FE | Status | Mask | Prescaler | Limit |

Status- status of device. There are flags:
b0- main counter is in PROCESS state (start pulse was received);
b7 – PLD version. For CGVI8 it is 0.
Mask – a mask register value.
Prescaler – a prescaler register value.

Limit – a limit register value. This byte is valid only if hardware version is not 1 and software version is above 4.

**FF** - device attribute request. There is not additional parameters. In reply a device sends the following message:

| FF | Device Code | HW version | SW version | Reason |
|---|---|---|---|---|

Device Code- device type (for CGVI8 it is equal 6).
HW version- hardware version of device.
SW version- software version of device.
Reason- reason of sending this message:

0- After power-up.
1- After reset by button on front panel.
2- On request by address message with code FF.
3- On request by broadcast message (who is here?).
4- On restart by Watchdog timer.
5- On busoff recovery.

The device sends this message on power-on.

### BROADCAST messages

For broadcast messages all devices analyze only field 1 in CANbus identifier. Valid combination is 5. A first byte of date presents a broadcast command. CGVI8 uses the only broadcast command:

FF- request "Who is here". On this broadcast request all devices on-line must send into network message with their attributes (and identifier).

## 6. Software versions for CGVI-8

There will be described modifications for software versions beyond 3st.

### Version 4.

1. There was "device type"=1 in "Busoff recovery" message. It is corrected.

### Version 5.

1. Prescaler register is 4 bits instead of 3.
2. Limit register is implemented.

******New functions are valid only with hardware revision 2 or above.**