TC3097-8

LITE END MULTIPORT REPEATER INTERFACE CONTROLLER

TAMARACK M. I.
4FL No. 106 Hsin-Tai Wu Road,
Sec. 1, Hsichih,
Taipei Hsien, Taiwan R.O.C.
TEL: 886-2-2696-1669
FAX:886-2-2696-2220

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Lite End Multiport Repeater Interface Controller

1. Features

- Functionally conforms to IEEE 802.3, Section 9, specification.
- 9 network connection(ports) per chip including:
  1 AUI PORT with fully compatible and drive capability(50m AUI cable).
  8 TP PORT with fully compatible and drive capability(100m TP cable).
- Cascadable for large multiple LEMRIC hub applications.
- On-chip Elasticity buffer, Manchester encoder and decoder.
- Separate partition state machine for each port.
- Embeded LED output driver for per port partition status, per port link/receive status(TP port), global jam status, and global jabber status. No external glue logic require.
- Embedded predistortion resistors for every TP port.
- Build in power reset circuit, no extra glue logic required.
- Crystal/Oscillater optional applicable.
- Manchester code violation detection and reporting.
- Support MAU Jabber Lockup Protection function.
  Support Auto Partition/Reconnection function to isolate a faulty segment's collision activity.
- Fully integrated Link Test logic with enable/disable option, conforming to the 10BASE-T standard.
- Fully integrated polarity detect/correct logic with enable/disable option for per TP port.
- Low power consumption , fully load < 900 mW.
- CMOS device feature high integration with a single + 5V supply.
- 100-pin QFP package.

2. General Description

The TC3097 Lite End Multiport Repeater Interface Controller (LEMRIC) may be used to implement an IEEE 802.3 multiport repeater unit. It fully satisfies the IEEE 802.3 repeater specification including the functions defined by the repeater, segment partition and jabber lockup protection state machines.
The LEMRIC has an on-chip phase-locked-loop (PLL) for Manchester data decoding, a Manchester encoder, and an Elasticity Buffer for preamble regeneration. In addition, it provides direct LED display driver pins for per port LINK/RCV status, per port partition jabber status, global jam and jabber lockup status indications.
Each LEMRIC can connect up to 9 cable segments via its network interface ports. One port is fully Attachment Unit Interface (AUI) compatible and is able to connect to an external Medium Attachment Unit (MAU) using the maximum length of AUI cable. The other 8 ports have integrated 10BASE-T transceivers. In addition, large repeater units may be constructed by cascading LEMRICs together over the Inter-LEMRIC bus.

3. Pin Description

Network Interface Pins (1 of 2)

Symbol	Pin No.	I/O	Description
RXI2A to RXI9A	42,46,58,64, 68,74,83,88	I	Twisted-Pair Receive Input Positive
RXI2B to RXI9B	43,47,59,65, 69,75,84,89	I	Twisted-Pair Receive Input Negative
TXO2RA to TXO9RA	45,50,56,62, 66,72,81,86	O	Twisted-Pair Transmit Output Positive
TXO2RB to TXO9RB	44,49,57,63, 67,73,82,87	O	Twisted-Pair Transmit Output Negative

Network Interface Pins (2 of 2)

Symbol	Pin No.	I/O	Description
RX1A	38	I	AUI Receive Input Positive
RX1B	39	I	AUI Receive Input Negative
TX1A	40	O	AUI Receive Output Positive
TX1B	41	O	AUI Receive Output Negative
CD1A	34	I	AUI Collision Detect Input Positive
CD1B	36	I	AUI Collision Detect Input Negative

Power & Ground Pins

Symbol	Pin No.	I/O	Description
GND	61,71,79	P	Ground pins for TP port 1 to port 8 output pins.
VDD	48,60,70,85	P	Power pins for TP port 1 to TP port 8 output pins.
GND	51,90,100	P	Ground pin for internal digital circuit of this device.
VDD	37,55,76,80	P	Power pin for internal digital circuit of this device.
GND	2,14,24	P	Ground pins for digital output pins.
VDD	1,27	P	Power pins for digital output pins.
AGND	45	P	Ground pin for PLL decoder internal circuit.
AVDD	39,40	P	Power pin for PLL decoder internal circuit.

Inter-LEMRIC Bus Pins (1 of 2)

Symbol	Pin No.	I/O	Description
ACKI	19	I	ACKnowledge Input: Input to the network port's arbitration chain.
ACKO	18	O	ACKnowledge Output: Output from the network port's arbitration chain.
IRD	16	B,Z	Inter-LEMRIC Data: When asserted as an output this signal provides a serial data stream in NRZ format. This signal is asserted by a LEMRIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-LEMRIC bus.
IREZ	15	B,Z	Inter-LEMRIC Enable: When asserted as an output this signal provides an activity framing enable for the serial data stream. The signal is asserted by a LEMRIC when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the inter-LEMRIC bus.
IRC	17	B,Z	Inter-LEMRIC Clock: When asserted as an output this signal provides a clock signal for the serial data stream. Data (XIRD) is changed on the falling edge of the clock. The default condition of this signal is to be an input. When an input, XIRD is sampled on the rising edge of the clock. In this state it may be driven by other devices on the Inter-LEMRIC bus.

Inter-LEMRIC Bus Pins (2 of 2)

Symbol	Pin No.	I/O	Description
COLNZ	22	B,Z	COLlision on Port N: This denotes that a collision is occurring on the port receiving the data packet (Port N). The default condition of this signal is to be an input. In this state it may be driven by the other devices on the Inter-LEMRIC bus.
ACTNZ	20	B,Z	ACTivity on Port N: This is a bi-directional signal. The LEMRIC asserts this signal when data or collision information is received from one of its network segments. The LEMRIC senses this signal when this or another LEMRIC in a multi-LEMRIC system is receiving data or collision information.
AYXNZ	21	B,Z	ACTivity on ANY Port Excluding Port N: This is a bidirectional signal. The LEMRIC asserts this signal when a transmit collision is experienced or multiple ports have active collisions on their network segments. The LEMRIC senses this signal when this LEMRIC or other LEMRICs in a multi-LEMRIC system are experience transmit collision or multiple ports have active collisions on their network segments.

LED Driver Pins (1 of 2)

Symbol	Pin No.	I/O	Description
COLED	3	O	Global Collision LED (Active-Low): This CMOS output indicates the status of the LEMRIC's any collision activity.
JABLED	4	O	Global Jabber LED (Active-Low): This CMOS output indicates when the LEMRIC's watchdog timer begins jab and stays active until end of the unjab wait period.
LRLED2 to LRLED9	6-13	O	Link/Receive LED (active-Low): This CMOS output goes active when the link integrity test is pass on LEMRIC's TP port network segment and blinks when this device is receiving from its link passing TP port segment.
LRLED1	5	O	AUI Receive LED (Active-Low): This CMOS output is power on active and blinking when this device is receiving from its AUI port network segment.
PALED1 to PALED9	91-99	O	Port Partition Jabber LED (Active-Low): This CMOS output goes active when the LEMRIC's network connection port is partitioned from its network segment and then goes inactive when its network connection port is reconnection from its network segment.

TEST Support Pins

Symbol	Pin No.	I/O	Description
TEST1 TEST3 TEST4	28 29 30	B	These pins are used to facilitate device testing. When not in test mode, these pins should be left open. [note:] Pins TEST3 and TEST4 can be used to modify the build in 10BASE-T operation. TEST1 can be used to configure LED display mode (TMI or AMD compatible mode). Detail refer to port Block Function section.

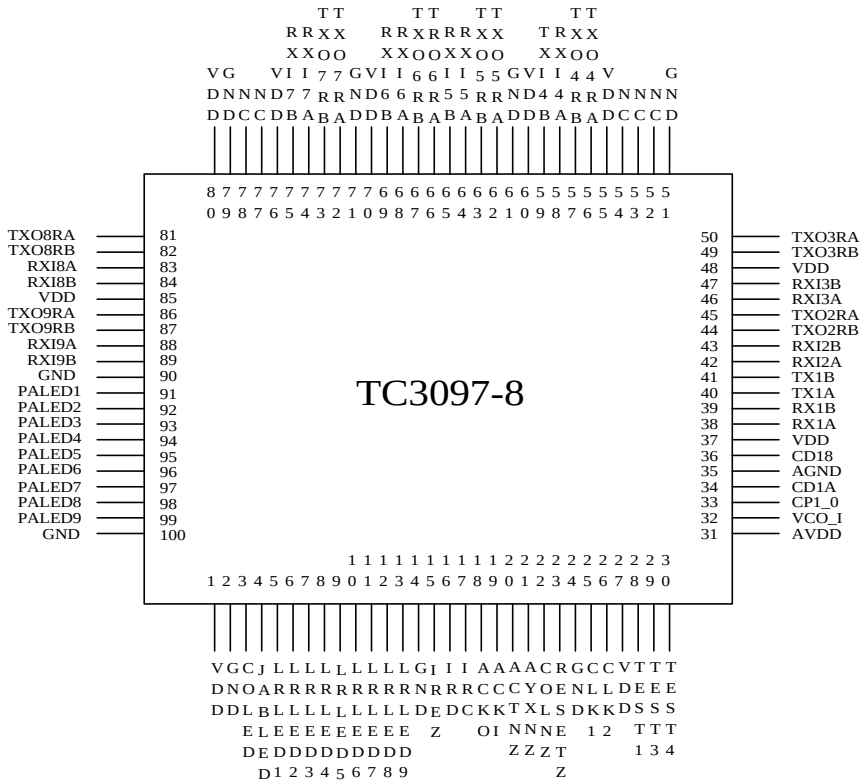
RESET & CLOCK Pins

Symbol	Pin No.	I/O	Description
RESETZ	23	I	Optional device Reset. A low on this pin causes the device to reset. RESET must be high for normal operation, when not used, please leave open.
CLK1 CLK2	25 26	I O	System Clock. 20 MHZ, 50% nominal, 40/60% worst case, duty cycle. The worst case frequency tolerance and duty cycle are to limit the range over which the LEMRIC will operate correctly. However, since this clock is used for Manchester data transmission, jitter performance will degrade if clock sources with relatively large tolerances are used.

Decoder Filer Pins

Symbol	Pin No.	I/O	Description
CP1_O	33	I	Phase Lock Loop delay line external filter. This pin should be connected correctly with a capacitor to ground or causing the analog PLL of the device to be fail.
VCO_I	32	I	Phase Lock Loop VCO external filter. This pin should be connected correctly with a RC filter circuit to ground or causing the analog PLL of the device to be fail.

TC3097-8 Connection Diagram



4. Principles Of Operation

4.1 Reset

The LEMRIC resets when XRESETZ (pin 25) is pulsed low. While reset. the LEMRIC ignores all energy and collision inputs, unjabs all ports, and initializes all timers, counters, and state machines. At the end of reset (XRESETZ goes high), all the LED's are turned off and the XLRLED1 is turned on.

The minimum XRESETZ low pulse is 1 second to let the power on LED test is visual distinguishable. The LEMRIC is fully operational when it exits reset.

4.2 Clock and data Recovery

The clock and data recovery circuit (Manchester decoder) is a linear circuit which recovers the NRZ data and clock from the Manchester encoded serial data stream. data from the active port is routed to the decoder and the recovered data is written into the FIFO.

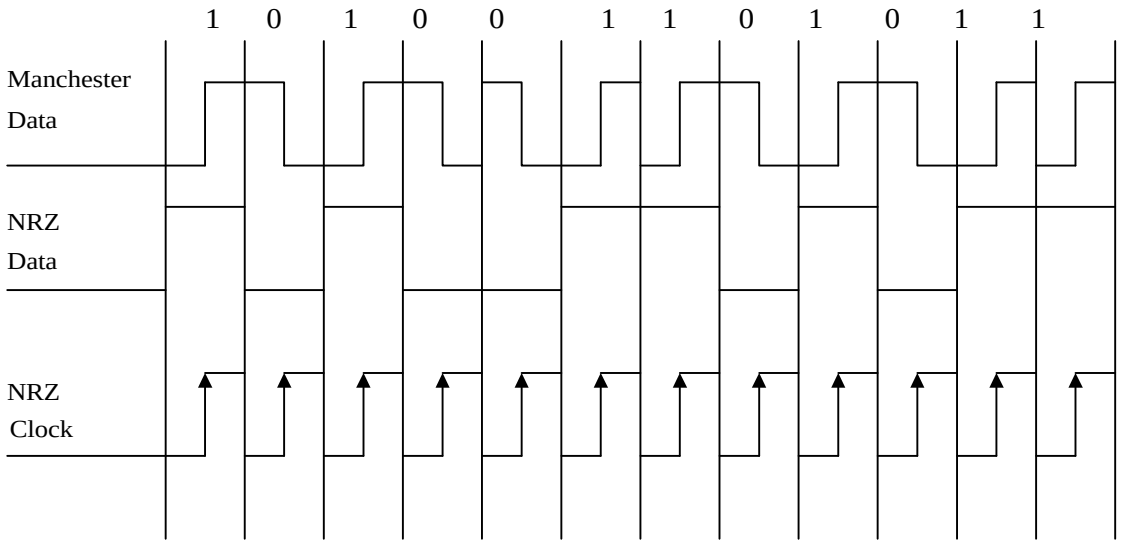


Figure 1. Manchester Data - NRZ Data Relationship

4.3 Functional State diagrams

The following state diagrams describe the auto-partition and global state machines implemented in the LEMRIC. The notation and variables used in each diagram are described below.

4.3.1 TP Port Auto-Partition State Diagram

A partitioning state machines is implemented for each TP port. individual Tw5 and Tw6 timers and collision counters are implemented for each state machine.

4.3.1.1 State Diagram Notation and Variables.

=	Assign the right side constant or expression result to the left side variable.
&	Logical "AND" operator.
+	Logical "OR" operator when used in a state-exiting expression. Arithmetic addition when used otherwise.
{[term]}	Group term for logical evaluation.
X	Number identifier for the particular TP port. Values : Integers from 1 to 8
CC(X)	Consecutive collision count for TP port X. Values : Integers from 0 to 31
DIPresent(X)	Carrier from the MAU on TP port X. Values : Idle-Port carrier is not active. Active-Port carrier is active.
Datain(X)	TP port X carrier to the global state machine. Values : Idle-Port carrier has been gated off by the partition state machine. DIPresent(X)-Port carrier is passed on to the global state machine.
TEN(X)	Status of transmission to the MAU on TP port X. Values : Idle-Not transmitting to the port MAU. Active-Transmitting to the port MAU.
/COLN	Inter-LEMRIC that is Port N or Port M collision. Values : Idle-/COLN is not active. Active-/COLN is active.
/ANYXN	Inter-LEMRIC that is not Port N or Port M collision. Values : Idle-/ANYXN is not active. Active-/ANYXN is active.
Tw5	Enable Tw5 initializes and starts the PORT Tw5 timer. Tw5Done indicates that the timer has expired.
Tw6	Enable Tw6 initializes and starts the port Tw6 timer. /Tw6Done indicates that the timer is running. Tw6Done indicates that the timer has expired.

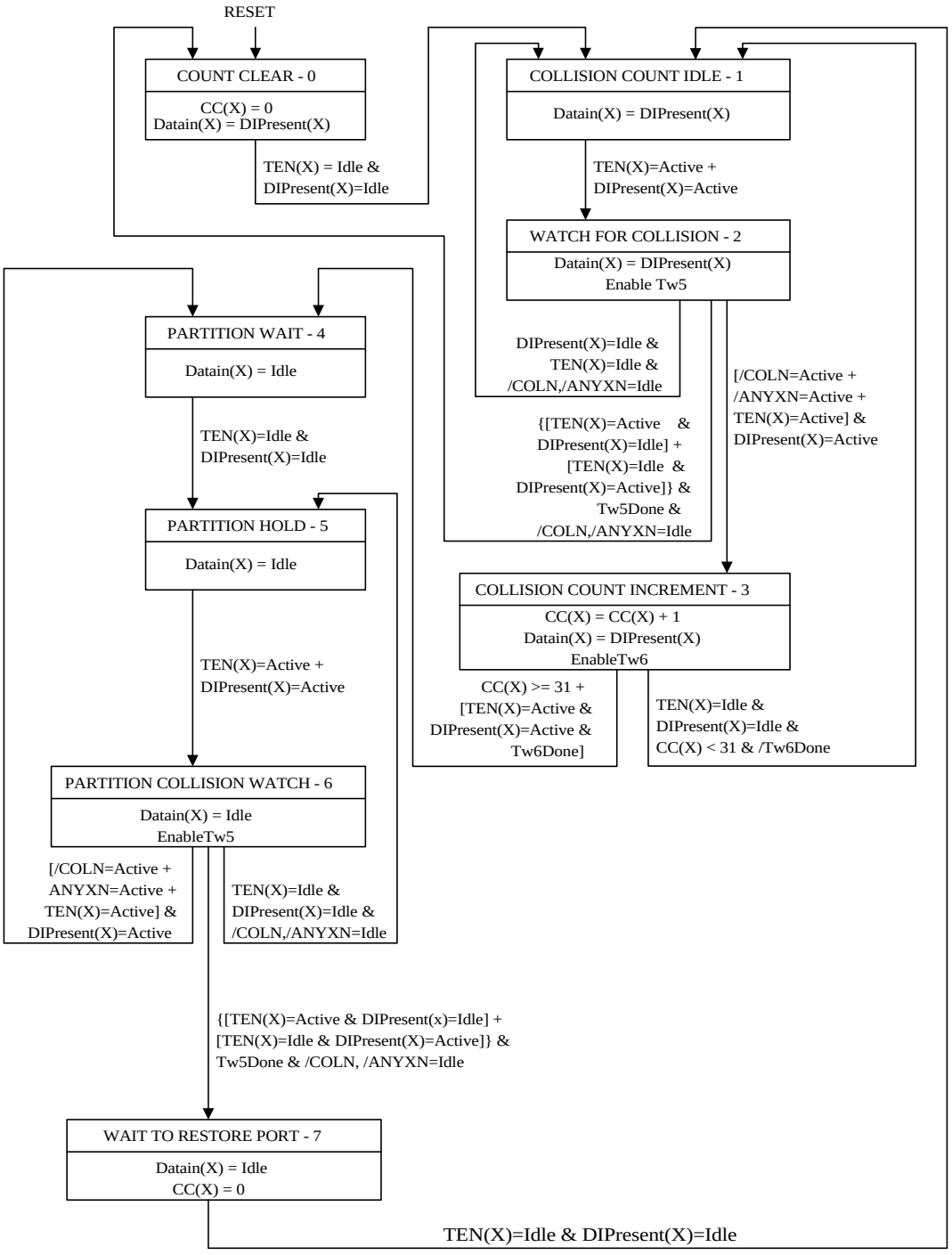


Figure 2. Partition State Diagram for TP Port X

4.3.2 AUI Port Auto-Partition State Diagram

A partition state machine is implemented for each AUI port. Individual Tw5 and Tw6 timers and collision counters are implemented for each state machine.

4.3.2.1 State Diagram Notation and Variables.

=	Assign the right side constant or expression result to the left side variable.
&	Logical "AND" operator.
+	Logical "OR" operator when used in a state-exiting expression. Arithmetic addition when used otherwise.
{[term]}	Group term for logical evaluation.
Y	Number identifier for the particular AUI port. Values : Integers 0 and 1
CC(Y)	Consecutive collision count for AUI port Y Values : Integers from 0 to 31
DIPresent(Y)	Carrier from the MAU on AUI port Y. Values : Idle-Port carrier is not active. Active-Port carrier is active.
Datain(Y)	AUI port carrier to the global state machine. Values : Idle-Port carrier has been gated off by the partition state machine. DIPresent(Y)-Port carrier is passed on to the global state machine.
CIPresent(Y)	Collision indication from the MAU on AUI Port Y. Values : /SQE-Port collision is not active. SQE-Port collision is active.
Collin(Y)	AUI port collision to the global state machine. Values : /SQE-Port collision has been gated off by the partition state machine. CIPresent(Y)-Port collision is passed on to the global state machine.
/COLN	Inter-LEMRIC that is Port N or Port M collision. Values : Idle-/COLN is not active. Active-/COLN is active.
/ANYXN	Inter-LEMRIC that is not Port N or Port M collision. Values : Idle-/ANYXN is not active. Active-/ANYXN is active.

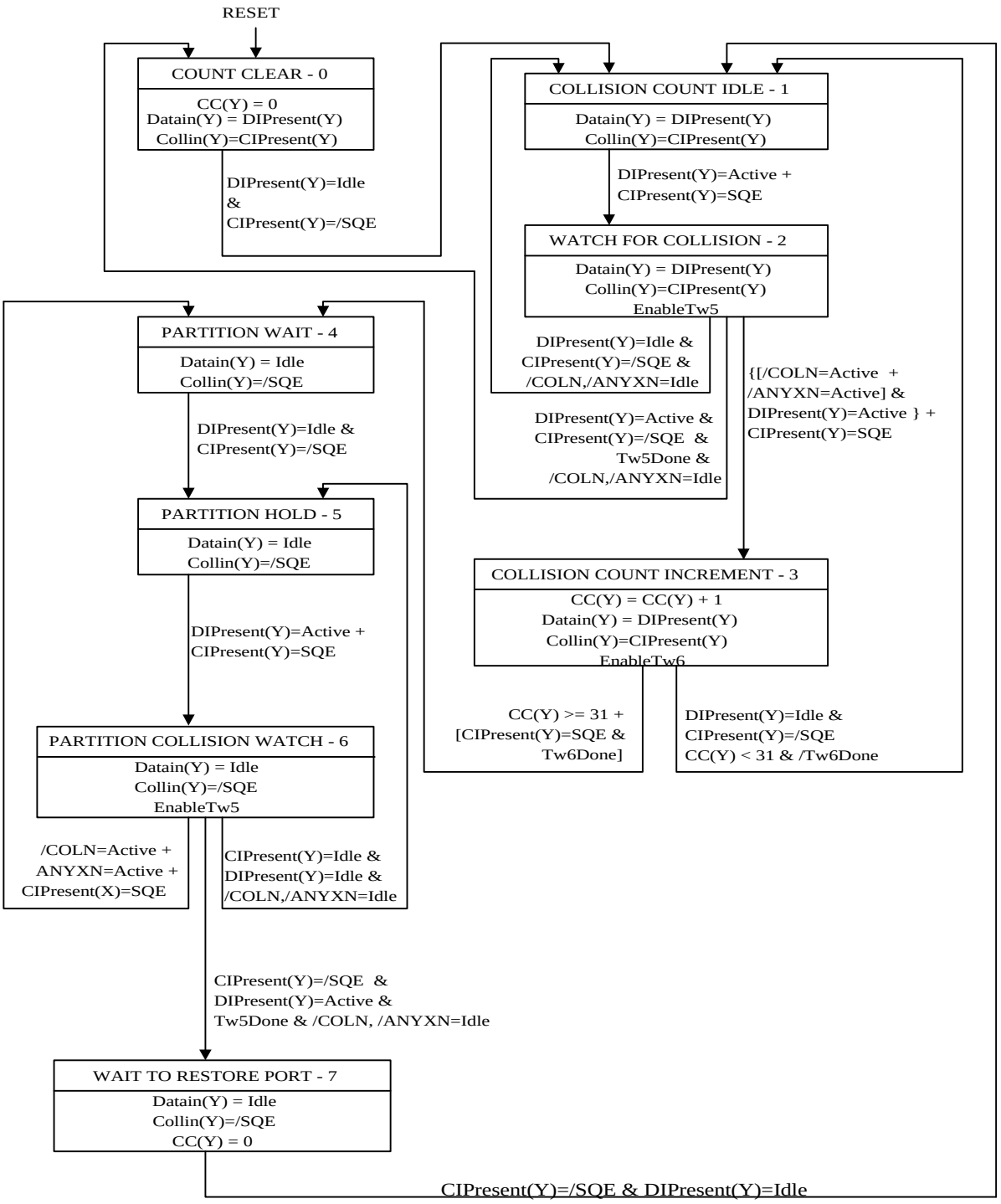


Figure 3. Partition State Diagram for AUI Port Y

Tw5	Enable Tw5 initializes and starts the PORT Tw5 timer. Tw5Done indicates that the timer has expired.
Tw6	Enable Tw6 initializes and starts the port Tw6 timer. /Tw6Done indicates that the timer is running. Tw6Done indicates that the timer has expired.

4.3.3 Global State Diagram

A single global state machine is implemented for the LEMRIC and operates independently of the auto-partition state machines. The machine state can be read externally on three pins when XRESETZ is high. The table below defines the values assigned to these pins for each state.

XTEST2/GS2	XTEST1/GS1	XTEST0/GS0	State	State Name
0	0	0	0	Idle
0	0	1	1	Send Data
0	1	1	3	Receive Collision
1	0	0	4	Transmit Collision
1	0	1	5	One Port Left
1	1	0	6	Blind

4.3.3.1 State Diagram Notation and Variables.

=	Assign the right side constant or expression result to the left side variable.
&	Logical "AND" operate.
+	Logical "OR" operator.
:	Denotes that a variable assignment expression follows.
<	Denotes assignment of the expression result following the arrow to the variable preceding the arrow.
{[term]}	Group term for logical evaluation.
Tw1	Enable Tw1 initializes and start the global Tw1 timer. Tw1Done indicates that the timer has expired.
Tw2	Tw2Done indicates that the Tw2 timer has expired.
AllDatatSent	Flag indicating that all the received bits have been sent.
OUT(P)	Type of output the LEMRIC is sending to port P. Values : Idle-The LEMRIC is not transmitting. Data-The LEMRIC is sending Preamble, data or IDL to port P. Jam-The LEMRIC is sending Jam to port P.
Datain(P)	Status of port P carrier. All AUI and TP ports are considered. Values : Idle-Port P carrier is not active. Active-Port P carrier is active.
Collin(P)	Status of AUI collision on port P. Values : /SQE-Port P collision is not active. SQE-Port P collision is active.
TT(P)	Indicates the number of bits transmitted to port P. Values : Positive integers.
Port(test)	Function that returns the identifier of a port passing test. For example, Port (TPDatain=Active) returns an integer identifying the active TP port. If more than one port passes the test, Only one of the acceptable values is returned. Values : Integers from 0 to 8

N	N is defined by the Port function (see above). It identifies the port that caused an exit from the ldle state to the Send Data or Receive Collision states.
M	M is defined by the Port function (see above). It identifies the single port that caused an exit from the Transmit Collision to the One Port Left state. Values : Integers from 0 to 8.
ONLY1	General test which is true if one and only one port is active due to carrier or collision. All TP and AUI ports are considered.
>1	General test which is true if greater than one port is active due to carrier or collision. All TP and AUI ports are considered.
ANY	General test which is true if one or more ports are active due to carrier or collision. All TP and AUI ports are considered.
ANYXN	General test which is true if any port other than port N meets the test condition. For example, TT(ANYXN) < 96 is true if a port other than port N was soured with fewer than 96 bits. All TP and AUI ports are considered.
ANYXM	General test which is true if any port other than port M is active due to carrier or collision. All TP and AUI ports are considered.
ALLXN	General test which is true if all ports other than port N meet the test condition. For example TT(ALLXN) > = 96 is true if all ports other than port N were soured with at least 96 bits. All TP and AUI ports are considered.
ALLXM	General test which is true if all ports other than port M meet the test condition. All TP and AUI ports considered.

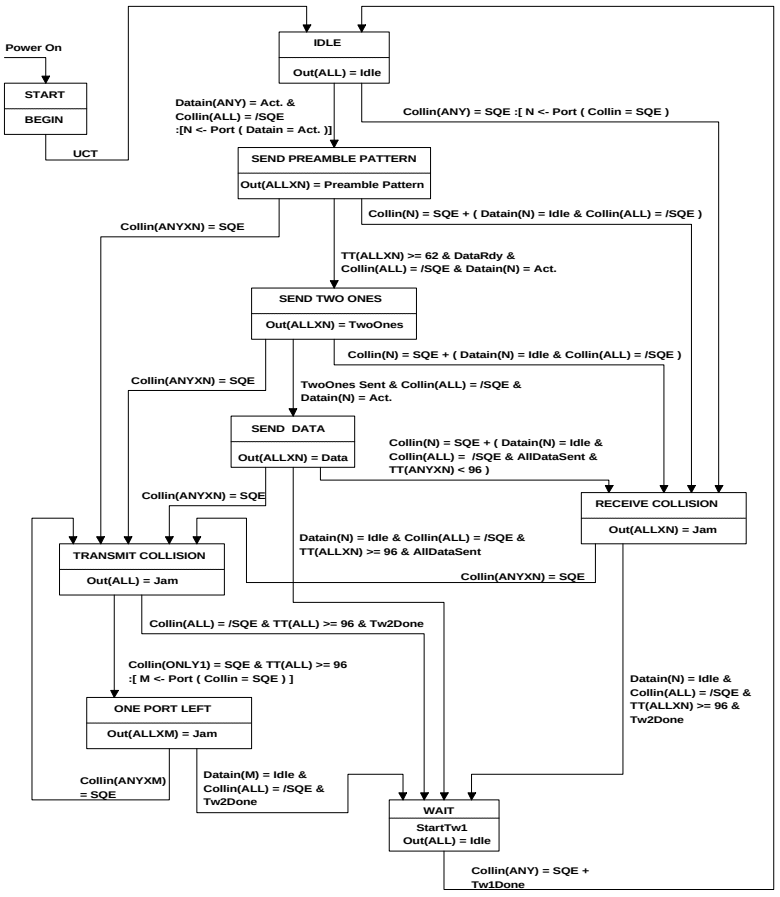


Figure 4. Global State Diagram for Multiple TP Ports and AUI Port

4.3.4 Counters and Timers

The counters and timers specified on IEEE 802.3. Section 9, are implemented in the LEMRIC. The function and values chosen for each is described below.

4.3.4.1 Tw1

Tw1 is the wait timer for the end of transmit recovery time and is 8 bit-times in duration. It is started when the LEMRIC ends transmission of a packet and prevents the LEMRIC from receiving this transmission (loop-back energy from the MAU) as a new receive entity.

4.3.4.2 Tw2

Tw2 is the wait timer for the end of carrier recovery time and is 3 bit-times in duration. It is started when collision on AUI port has ended. Tw2 prevents the LEMRIC from premature detecting the true end-of-collision due to signal uncertainty on the segment at the end of a collision.

Refer to the following figure. If a collision (SQE) is detected on AUI segment, the Tw2 timer becomes armed. Tw2 begins timing when collision is idle (/SQE). After Tw2 is done, the timer remains idle until the next AUI collision.

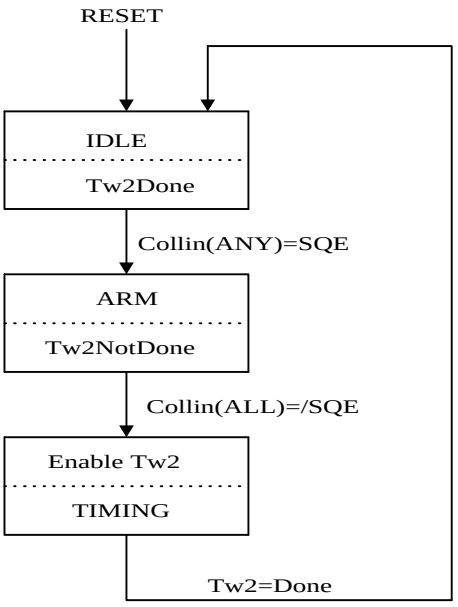


Figure 5. Tw2 State Diagram.

4.3.4.3 Tw3

Tw3 is the wait timer for length of continuous output and is 65536 bit-times in duration. It is started when transmission of a packet begins. If Tw3 expires before transmission of he packet ends, the LEMRIC enters the MAU jabber lockup protection condition and interrupts transmission for period Tw4. Refer to the figure below.

4.3.4.4 Tw4

Tw4 is the wait timer for time to disable output for MAU jabber lockup protection and is 96 bit-times in duration. It is started when Tw3 expires. While Tw4 is active, transmission to all ports is disabled. the global state machine is reset to the Idle state, the FIFO controller is reset, and the clock recovery circuit continues to decode the incoming data stream. If the port is still active when Tw4 expires, the LEMRIC will resume transmission beginning with preamble.

The MAU lockup LED (XJABLED) is turned on to indicates the suspension of transmission. Refer to the following figure.

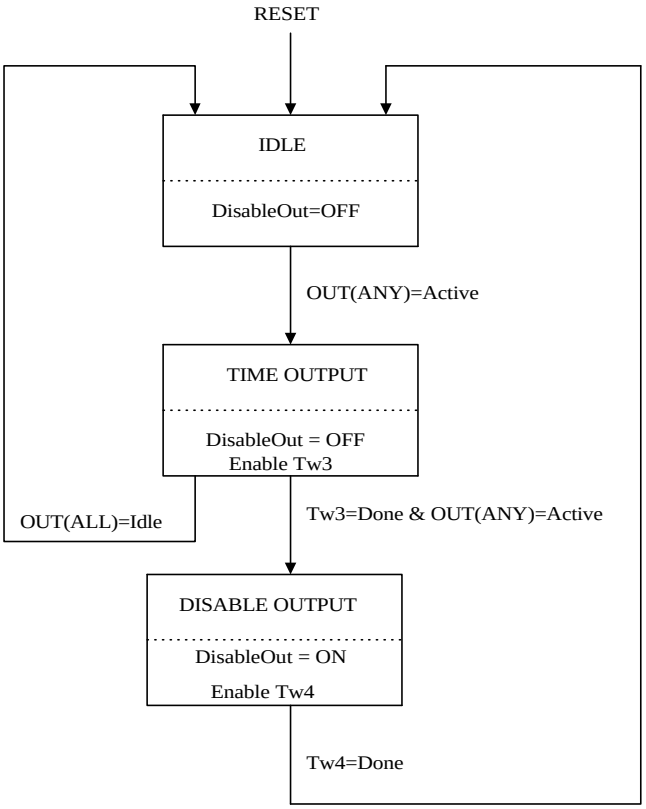


Figure 6. MAU jabber Lockup Protection State Diagram

4.3.4.5 Tw5

Tw5 is the auto-partition wait timer for length of packet without collision and is 512 bit-times in duration. It is started when carrier (or collision on AUI ports) from a port becomes active. If a collision is detected before Tw5 expires, the collision count for that port is incremented and the port Tw6 timer is started. Tw5 is also used in the auto-partition algorithm to exit the Partition collision Watch state. A separate Tw5 timer is implemented for each of the TP and AUI ports.

Refer to the auto-partition state diagrams for specific timer operation.

4.3.4.6 Tw6

Tw6 is the auto-partition wait timer for excessive length of collision and is 1024 bit-times in duration. It is started if a collision (multiple active port or SQE) is detected before Tw5 expires. If the collision condition persists when Tw6 expires. The energy and data from that port are partitioned (jabbed). A separate Tw6 timer is implemented for each of the TP and AUI ports.

Refer to the auto-partition state diagrams for specific timer operation.

4.3.4.7 Collision counter

The collision counter maintains the number of consecutive collisions for a particular port. If the collision limit is reached, the energy and data from that port are partitioned (jabbed). A separate collision counter with limit 31 is implemented for each of the TP and AUI ports.

4.3.4.8 Transmit Timer

The transmit timer counts the number of bits transmitted to a port. If the total number of bits transmitted is less than 96 (due to reception of a packet fragment). The LEMRIC will enter the Receive Collision global state and transmit Jam until the transmit timer reaches a count of 96. there by extending the bit stream to > = 96 bits.

The transmit timer is cleared when the LEMRIC enters the Transmit Collision global state. This ensures that at least 96 bits of Jam are transmitted to all ports before the LEMRIC exits the Transmit Collision state. This also means that the LEMRIC will have transmitted more than 96 bits of Jam to all but one port if the transmit collision state was entered from the Receive collision state. Refer to the following figure and the global state diagram for transmit timer operation.

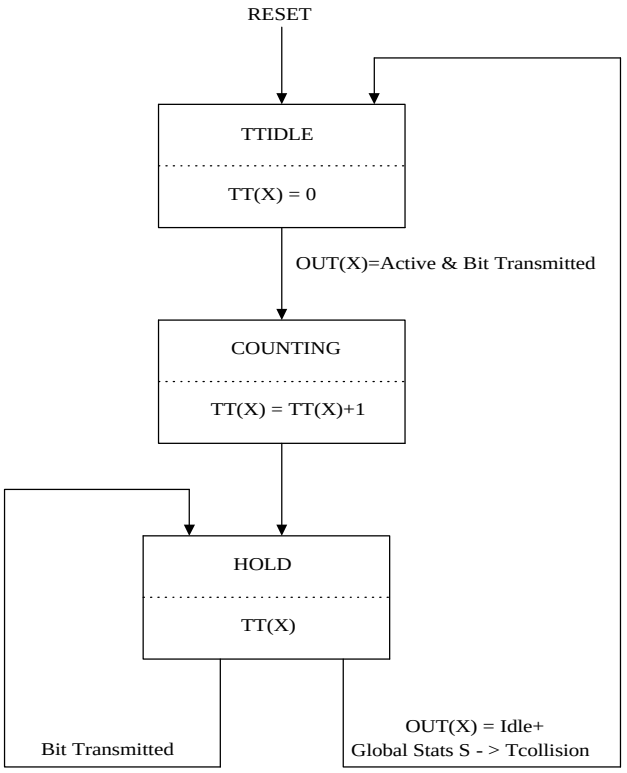


Figure 7. Transmit Timer State Diagram for Port X.

4.3.5 Automatic Preamble Regeneration

Automatic preamble regeneration (APRG) prevents the preamble from shrinking as a packet is passed from repeater to repeater or station to station. This shrinking, or loss of bits, is due to the bit cost of determing the presence of carrier and synchronizing of the Manchester data for NRZ data and clock recovery. The LEMRIC compensates for the bit loss by transmitting > = 56 bits of preamble before sending the Start of Frame Delimiter (SFD) pattern.

4.3.5.1 APRG Circuit Operation

When carrier is detected, the LEMRIC begins sending preamble and searches for the SFD pattern in the recovered NRZ data. The delay from carrier transition to the first transmitted bit of preamble is four to five bit-times for AUI carrier and eight to nine bit-times for TP carrier. The LEMRIC begins searching for the eight-bit SFD pattern 15 to 16 bits after the carrier transition.

When the SFD pattern is detected data following the SFD is loaded into a 64-bit FIFO. after the preamble bits are sent, the SFD pattern is sent, and then the FIFO data is sent. since at least 56 bits of preamble must be sent. the FIFO must be of sufficient depth to store the data after the SFD pattern. A FIFO depth of 64 is chosen to allow the processing of packet with very few bits of preamble before SFD.

The FIFO watermark is achieved by reloading the FIFO with part of the SFD pattern. A preamble counter maintains the number of preamble bits transmitted. and is implemented such that the total count equals 56 plus the number of SFD bits not reloaded into the FIFO. For a watermark of four bits, the preamble counter counts to 60 (56 preamble bits plus the first four bits of SFD). The received packet must contain at least 16 preambles bits for the LEMRIC to detect SFD. There is no upper limit on the number of preamble bits received.

The latency of bits through the LEMRIC is inversely related to the number of preamble bits received. That is the data in a packet with a small number (<56) of preamble bits must be stored (and therefore be held a longer period of time) until the full preamble can be regenerated.

For a packet with a large number (>=56) of preamble bits, the latency will approach the processing time of the LEMRIC (including watermark) to get a bit from the input through the FIFO to the output. If the number of preamble bits received is greater than 56, the LEMRIC will add up to four preamble bits to the packet for TP carrier and up to eight preamble bits for AUI carrier.

The leading edge of the first preamble bit transmitted by the LEMRIC, as seen on the line. Denotes the beginning of a 100 nanosecond positive (TTL logic one).

4.3.5.2 APRG State Diagram

The following state diagram describes the LEMRIC APRG operation. When carrier is detected, the APRG circuit waits from four to noise bit-times and then begins sending preamble, The preamble counter (PC) increments for each preamble bit sent. When the SFD pattern is detected (all eight bits), the data bits are loaded into the FIFO and the SFD pattern is sent. The error paths indicate some sort of packet abort, such as collision, Manchester code violation, FIFO error, or premature end of packet. The state diagram notation is similar to that of the global state diagram.

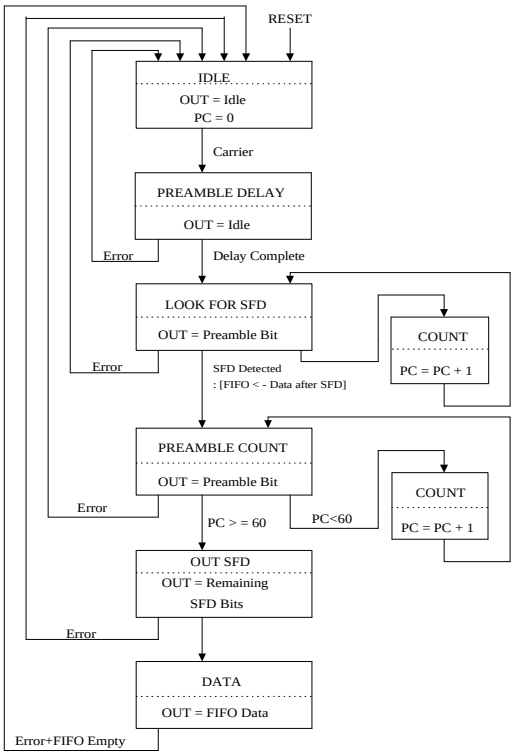


Figure 8. State Diagram for Automatic Preamble Regeneration

4.3.6 Inter-LEMRIC Bus Operation

The Inter-LEMRIC Bus, consists of eight signals. These signals implement a protocol which may be used to connect multiple LEMRICs together. In this configuration, the logical function of a single repeater is maintained. The resulting multi-LEMRIC system is compliant to the IEEE 802.3 Repeater Specification and may connect serval hundred network segments. An example of a multi-LEMRIC system is shown as follow below:

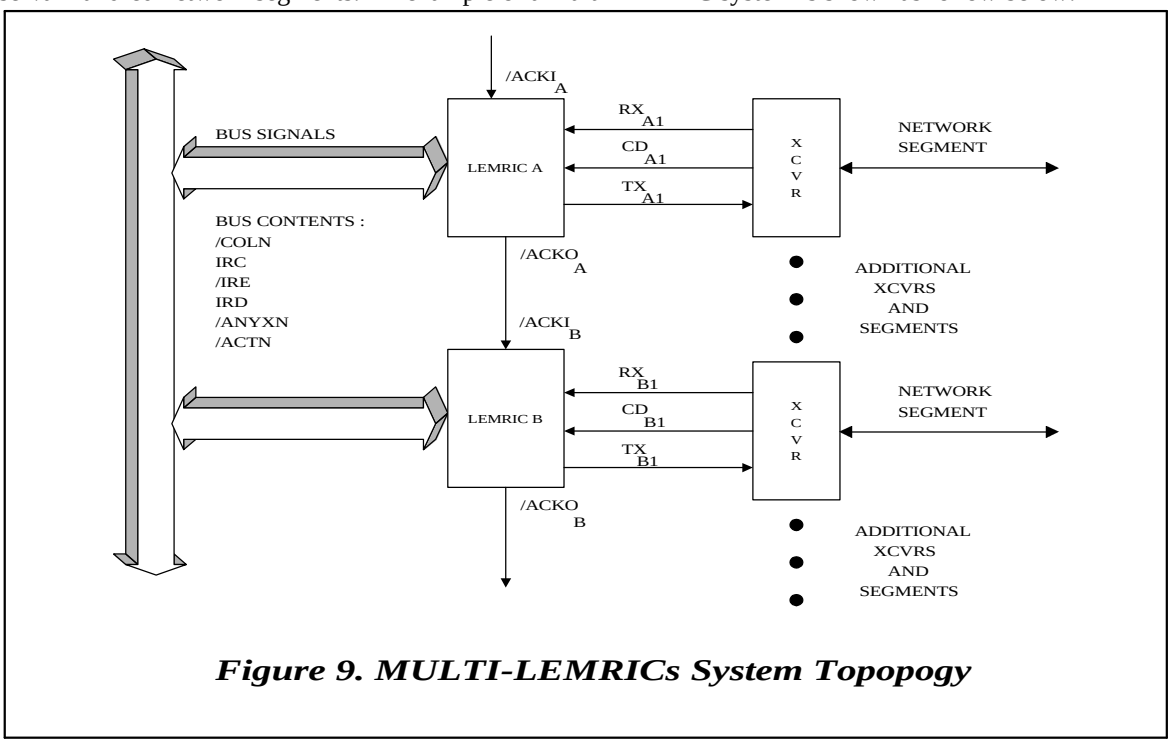


Figure 9. MULTI-LEMRICs System Topopogy

The Inter-LEMRIC bus connects multiple LEMRICs to realize the following operations:

- Port N Identification (which port the repeater receives data from)
- Port M Identification (which port is the last one experiencing a collision)
- Data Transfer
- RECEIVE COLLISION Identification
- TRANSMIT COLLISION Identification
- DISABLE OUTPUT (jabber protection)

The following tables briefly describe the operation of each bus signal, the conditions required for a LEMRIC to assert a signal and which LEMRICs (in a multi-LEMRIC system) would monitor a signal:

ACKI

Function	Input signal to the Inter-LEMRIC arbitration chain. This chain is employed to identify PORT N and PORT M. • Note : LEMRIC which contains PORT N or PORT M may be identified by its ACKO signal being low when its ACKI input is high.
Conditions required for a LEMRIC to drive this signal	Not Applicable
LEMRIC Receiving the Signal	This is dependent upon the method used to cascade LEMRICs, described in Section 1.3.6.2.

ACKO

Function	Output signal from the Inter-LEMRIC arbitration chain.
Conditions required for a LEMRIC to drive this signal	This is dependent upon the method used to cascade LEMRICs described in Section 1.3.6.2.
LEMRIC Receiving the Signal	Not applicable

/ACTN

Function	This signal denotes there is activity on PORT M.
Conditions required for a LEMRIC to drive this signal	A LEMRIC must contain PORT N or PORT M. • Note : Although this signal normally has only one source asserting the signal active it is used in a wired-OR configuration.
LEMRIC Receiving the Signal	This signal is monitored by all LEMRICs in the repeater system.

/ANYXN

Function	This signal denotes that a repeater port that is not PORT N or PORT M is experiencing a collision.
Conditions required for a LEMRIC to drive this signal	Any LEMRIC which satisfies the above condition. Note : This bus line is used in a wired-OB configuration.
LEMRIC Receiving the Signal	This signal is monitored by all LEMRICs in the repeater system.

/COLN

Function	Denotes PORT N or PORT M is experiencing a collision.
Conditions required for a LEMRIC to drive this signal	A LEMRIC must contain PORT N or PORT M.
LEMRIC Receiving the Signal	The signal is monitored by all other LEMRICs in the repeater system.

/IRE

Function	This signal acts as an activity framing signal for the IRC and IRD signals.
Conditions required for a LEMRIC to drive this signal	A LEMRIC must contain PORT N .
LEMRIC Receiving the Signal	The signal is monitored by all other LEMRICs in the repeater system.

/IRD

Function	Decoded serial data, in NRZ format, received from the network segment attached to PORT N.
Conditions required for a LEMRIC to drive this signal	A LEMRIC must contain PORT N .
LEMRIC Receiving the Signal	The signal is monitored by all other LEMRICs in the repeater system.

/IRC

Function	Clock signal associated with IRD and IRE.
Conditions required for a LEMRIC to drive this signal	A LEMRIC must contain PORT N .
LEMRIC Receiving the Signal	The signal is monitored by all other LEMRICs in the repeater system.

4.3.6.1 Methods of LEMRIC Cascading

In order to build multi-LEMRIC repeaters, PORT N and PORT M identification must be performed across all the LEMRICs in the system.

The top of the chain, the input to Port 1 is accessible to the user via the LEMRIC's /ACKI input pin. The output from the bottom of the chain becomes the /ACKO output pin. In a single LEMRIC system PORT N is defined as the port in the arbitration chain with receive or collision activity. PORT N identification is performed when the repeater is in the IDLE state. In order for the arbitration chain to function, all that needs to be done is to tie the /ACKI signal to a logic high state. In multi-LEMRIC systems there are two methods to propagate the arbitration chain between LEMRICs:

The first and most straightforward way is to extend the arbitration chain by daisy-chaining the /ACKI-/ACKO signals between LEMRICs. In this approach one LEMRIC is placed at the top of the chain (its /ACKI input is tied high), then the /ACKO signal from this LEMRIC is send to the /ACKI input of the next LEMRIC and so on. This arrangement is simple to implement but it places some topological restrictions upon the repeater system. In particular, when the repeater is constructed using a backplane with removable printed circuit boards containing the LEMRICs, If one of the boards is removed then the /ACKI-/ACKO chain will be broken and the repeater will not operate correctly.

The second method of PORT N or PORT M identification avoids this problem. This second technique relies on an external parallel arbiter which monitors all of the LEMRIC's /ACKO signals and responds to the LEMRIC with the highest priority. In this scheme each LEMRIC is assigned with a priority level. One method of doing this is to assign a priority number which reflects the position of a LEMRIC board on the repeater backplane (i.e., its slot number). When a LEMRIC experiences receive activity and the repeater system is in the IDLE state, the LEMRIC board will assert /ACKO. External arbitration logic drives the identification number onto an arbitration bus and the LEMRIC containing PORT N will be identified. An identical procedure is used in the TRANSMIT COLLISION state to identify PORT M. This parallel means of arbitration is not subject to the problems caused by missing boards (I. e., empty slots in the backplane). The logic associated with asserting this arbitration vector in the various in the various packet repetition scenarios could be implemented in PAL or GAL type devices.

To perform PORT N or PORT M arbitration, both of the above methods employ the same signals: /ACKI, /ACKO, and /ACTN.

The Inter-LEMRIC bus allows multi-LEMRIC operations to be performed in exactly the same manner as if there is only a single LEMRIC in the system. The simplest way to describe the operation of Inter-LEMRIC bus is to see how it is used in a number of common packet repetition scenarios.

4.3.6.2 EXAMPLES OF PACKET REPETITION SCENARIOS

Data Repetition

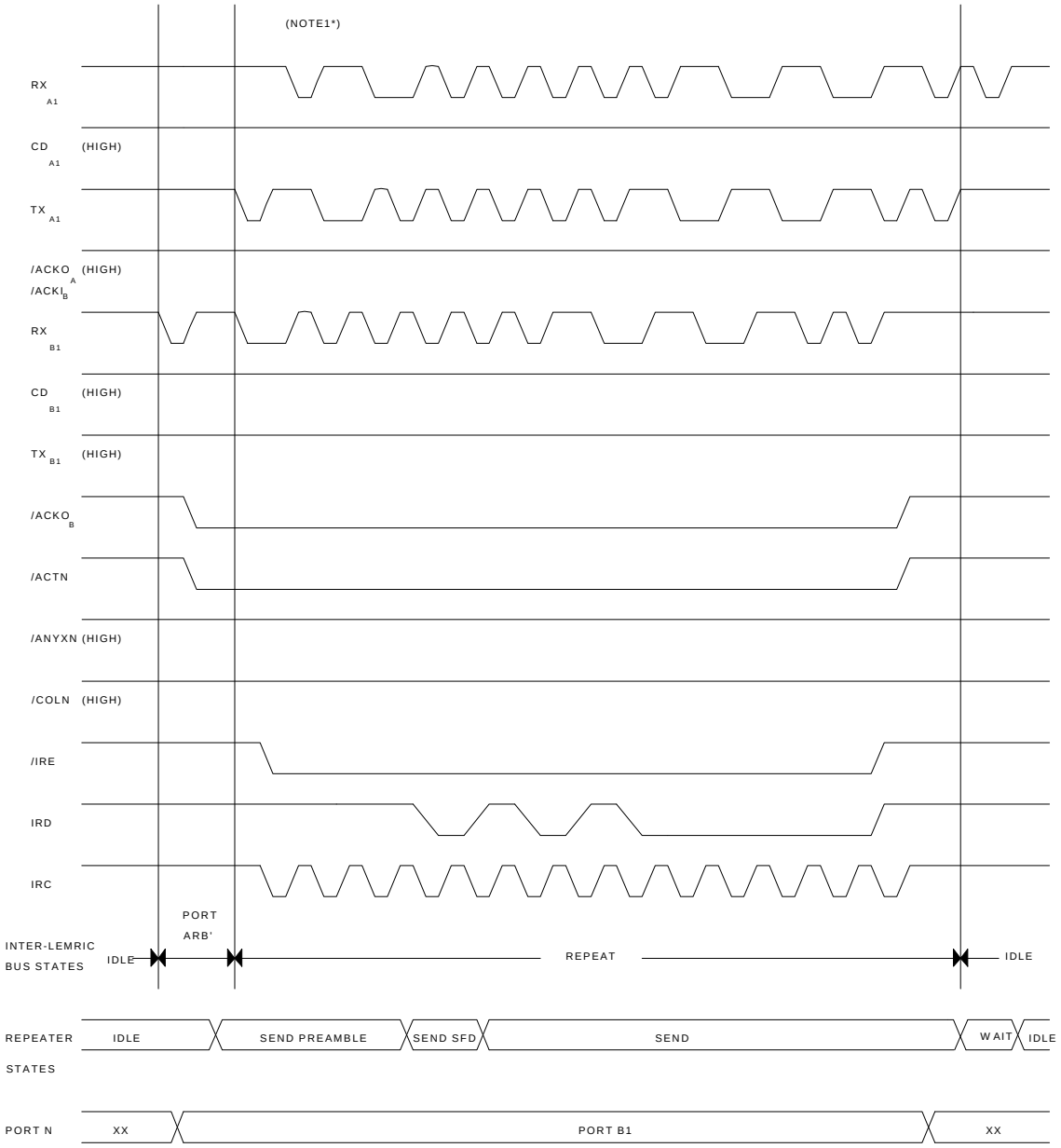
The simplest packet operation performed over the Inter-LEMRIC Bus is data repetition. In this operation a data packet is received at one port and transmitted to all other segments.

The first task to be performed is PORT N identification. In situations where two or more ports simultaneously receive packets the Inter-LEMRIC bus operates by choosing one of the active ports and forcing the others to transmit data. This is done to faithfully follow the IEEE specification's allowed exit paths from the IDLE state (I. e., to the SEND PREAMBLE PATTERN or RECEIVE COLLISION states).

The packet begins with a preamble pattern derived from the LEMRIC's on chip jam/preamble generator. The data received at PORT N is directed through the receive multiplexer to the PLL decoder. Once phase lock has been achieved, the decoded data, in NRZ format, with its associated clock and enable signals are asserted onto to IRD, /IRE and IRC Inter-LEMRIC bus lines, This serial data stream is received from the bus by all LEMRICs in the repeater and directed to their Elasticity Buffers. Logic circuit monitor the data stream and look for the Start of Frame Delimiter (SFD).

When this has been detected data is loaded into the elasticity buffer for later transmission. This will occur when sufficient preamble has been transmitted and certain internal state machine operations have been fulfilled.

Figure 11 shows two LEMRICs, A and B, daisy-chained together with LEMRIC A positioned at the top of the chain. A packet is received at port B1 of LEMRIC B and is then repeated by the other ports in the system. figure 12 shows the functional timing diagram for this packet repetition represented by the signals shown in figure 11. In this example only two ports in the system are shown, obviously the other port also repeat the packet. It also indicates the operation of the LEMRIC's state machines in so far as can be seen by observing the Inter-LEMRIC bus. for reference, the repeater's state transitions are shown in terms of the states defined by the IEEE specification. The location (I. e., which port it is) of PORT N is also shown. The following section describes the repeater and Inter-LEMRIC bus transitions shown in figure 10.



NOTE 1:The activity shown on RX A1 represents the transmitted signal on TX A1 after being looped back by the attached .

FIGURE 10. Data Repetition

The repeater is stimulated into activity by the data signal received by port B1. The LEMRICs in the system are alerted to forthcoming repeater operation by the falling edges on the /ACKI-/ACKO daisy chain and the /ACTN bus signal. following a defined start up delay the repeater moves to the SEND PREAMBLE state. The LEMRIC system utilizes the start up delay to perform port arbitration. When packet transmission begins the LEMRIC system enters the REPEAT state. The expected, for normal packet repetition, sequence of repeater states, SEND PREAMBLE, SEND SFD and SEND DATA is followed but is not visible upon the Inter-LEMRIC bus. They are merged together into a single REPEAT state. This is also true for the WAIT and IDLE states, they appear as a combined Inter-LEMRIC bus IDLE state.
Once a repeat operation has begun (I. e., the repeater leaves the IDLE state) it is required to transmit at least 96 bits of data or jam/preamble onto its network segments.
If the duration of the received signal from PORT N is smaller than 96 bits, the repeater transitions to the RECEIVE COLLISION state (described later). This behavior is known as fragment extension. After the packet data has been repeated, including the emptying g of the LEMRICs' elasticity buffers, the LEMRIC performs the Tw1 transmit recovery operation. This is performed during the WAIT state shown in the repeater state diagram.

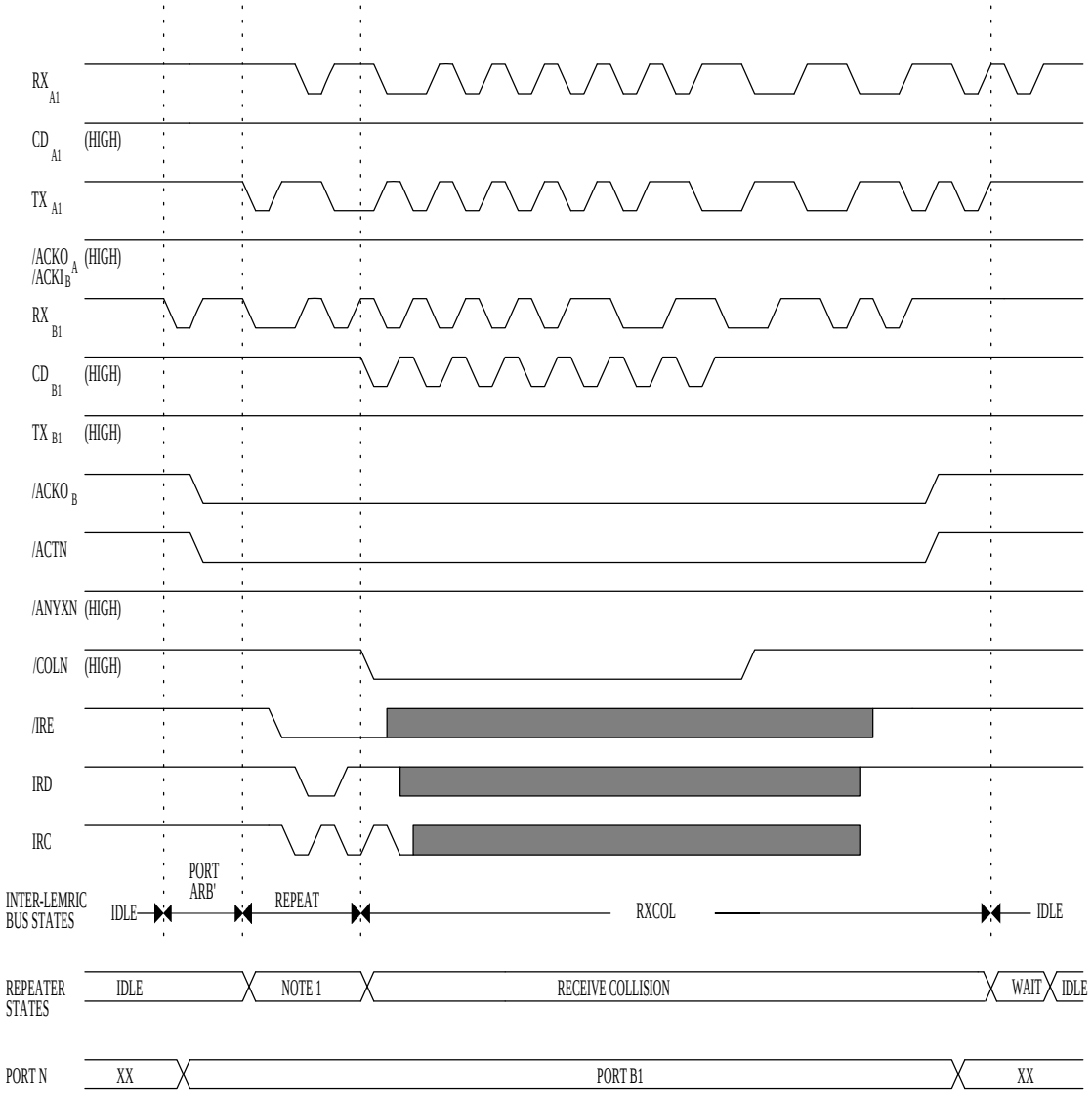
4.3.6.3 EXAMPLES OF PACKET REPETITION SCENARIOS

Receive Collisions
A receive collision is a collision which occurs on the network segment attached to PORT N (I. e., the collision is "received" in a similar manner as a data packet is received and then repeated to the other network segments). Not surprisingly, receive collision propagation follows a similar sequence of operations as is found with data repetition:
An arbitration process is performed to find PORT N and a preamble/jam pattern is transmitted by the repeater's other ports. When PORT N detects a collision on its segment the /COLN Inter-LEMRIC bus signal is asserted. This forces all the LEMRICs in the system to transmit a preamble/jam pattern to their segments. This is important since they may be already transmitting data from their elasticity buffers. The repeater moves to the RECEIVE COLLISION state when the LEMRICs begin to transmit the jam pattern. The repeater remains in this state until both the following conditions have been fulfilled:
1. At least 96 bits have been transmitted onto the network,
2. The activity has ended.

Under close examination the repeater specification reveals that the actual end of activity has its own permutations of conditions:
1. collision and receive data signals may end simultaneously,
2. Receive data may appear to end before collision signals,
3. Receive data may continue for some time after the end of the collision signal.

Network segments using coaxial media may experience spurious gaps in segment activity when the collision signal goes inactive. This arises from the inter-action between the receive and collision signal squelch circuits. Implemented in coaxial transceivers, and the properties of the coaxial cable itself. The repeater specification avoids propagation of these activity gaps by extending collision activity by the Tw2 wait time. Jam pattern transmission must be sustained throughout this period. After this, the repeater will move to the WAIT state unless there is a data signal being received by PORT N.

The functional timing diagram, figure 11, shows the operation of a repeater system during a receive collision. The system configuration is the same as earlier described and is shown in Figure 9.
The LEMRICs perform the same PORT N arbitration and data repetition operations as previously described. The system is notified of the receive collision on port B1 by the /COLN bus signal going active. This is the signal which informs the main state machines to output the jam pattern rather than the data held in the elasticity buffers. Once a collision has occurred the IRC, IRD and /IRE bus signals may become undefined. when the collision has ended and the Tw2 operation performed, the repeater moves to the WAIT state.



NOTE1 : SEND PREAMBLE, SEND SFD , SEND DATA

FIGURE 11. Receive Collision

4.3.6.4 EXAMPLES OF PACKET REPETITION SCENARIOS

Transmit Collisions

A transmit collision is a collision that is detected upon a segment to which the repeater system is transmitting. The state machine monitoring the colliding segment asserts the /ANYXN bus signal. The assertion of /ANYXN causes PORT M arbitration to begin. The repeater moves to the TRANSMIT COLLISION state when the port which had been PORT N starts to transmit a Manchester encoded 1 on to its network segment. While in the TRANSMIT COLLISION state all ports of the repeater must transmit the 1010... jam pattern and PORT M arbitration is performed. Each LEMRIC is obliged, by the IEEE specification, to ensure all of its ports transmit for at least 96 bits once the TRANSMIT COLLISION state has been entered. This transmit activity is enforced by the /ANYXN bus signal. while /ANYXN is active all LEMRIC ports will transmit jam. To ensure this situation lasts for at least 96 bits, the MSMs (Main state Machine) inside the LEMRICs assert the /ANYXN signal throughout this period. After this period has elapsed, /ANYXN will only be asserted if there are multiple ports with active collisions on their network segments.

There are two possible ways for a repeater to leave the TRANSMIT COLLISION state. The most straightforward is when network activity (I. e., collisions and their Tw2 extensions) end before the 96-bits enforced period expires. Under these conditions the repeater system may be move directly to the WAIT state when 96 bits have been transmitted to all ports. If the MSM enforced period ends and there is still one port experiencing a collision the ONE PORT LEFT state is entered. This may be seen on the Inter-LEMRIC bus when /ANYXN is reasserted and PORT M stops transmitting to its network segment. In this circumstance the Inter-LEMRIC bus transitions to the RECEIVE COLLISION state. The repeater will remain in this state while PORT M's collision, Tw2 collision extension and any receive signals are present. When these conditions are not true, packet repetition finishes and the repeater enters the WAIT state.

Figure 12 shows a multi-LEMRIC system operating under transmit collision conditions. There are many different scenarios which occur during a transmit collision, this figure illustrates one of these. This figure illustrates one of these. The diagram begins with packet reception by port A1. Port B1 experiences a collision, since it is not PORT N it asserts /ANYXN. This alerts the MSMs in the system to switch from data to jam pattern transmission. Port A1 is also monitoring the /ANYXN bus line. Its assertion forces A1 to relinquish its PORT N status, start transmission, stop asserting /ACTN and release its hold on the arbitration signals (/ACKO A and /ACKI B). The first bit it transmits will be a Manchester encoded "1" in the jam pattern.

Since port B1 is the only port with a collision, it attains PORT M status and stop asserting /ANYXN. It does however assert /ACTN, and exert its presence upon the arbitration chain (forces /ACKO B low). The MSMs ensure that /ANYXN stays active and thus forces all of the ports, including PORT M, to transmit to their segments.

After some time port A1 experience of the packet being received from port A1's segment plus the jam signal the repeater is now transmitting onto this segment. Two packets on one segment results in a collision. PORT M now moves from B1 to A1. Port A1 fulfills the same criteria as B1 (I. e., it has an active collision on its segment), but in addition it is higher in the arbitration chain.

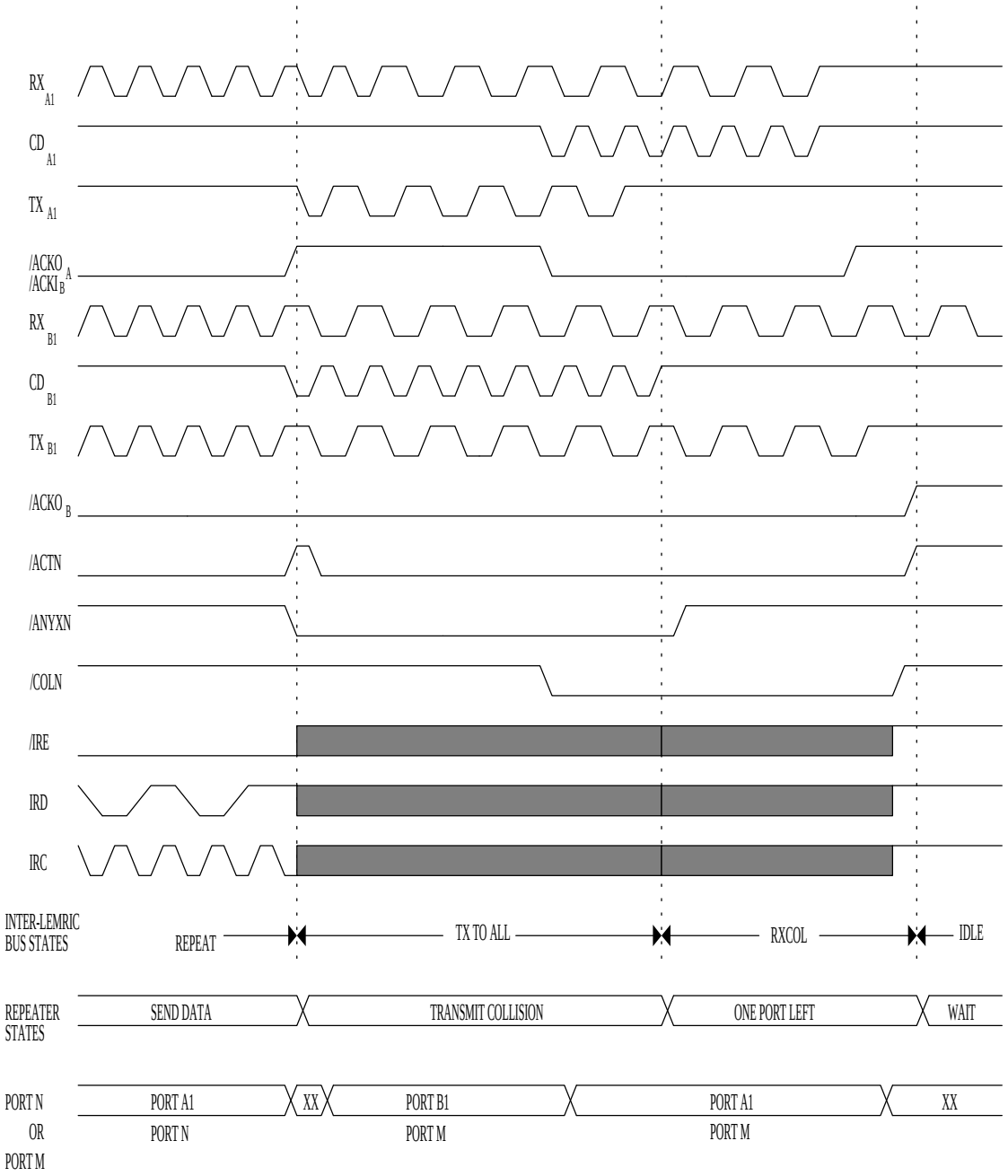


FIGURE 12. Transmit Collision

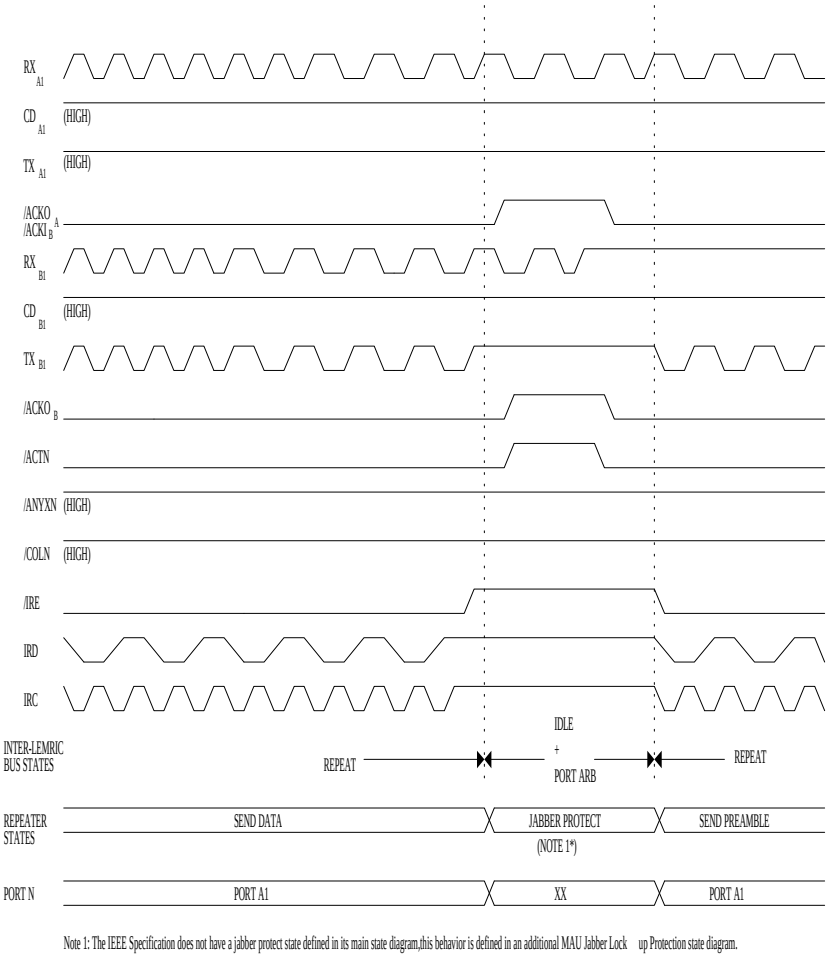
Eventually the collision on port B1 ends and the /ANYXN extension by the MSMs expires. There is only one collision on the network (this may be deduced since /ANYXN is inactive) so the repeater will move to the ONE PORT LEFT state. The LEMRIC system treats this state in a similar manner to a receive collision with PORT M fulfilling the role of the receiving port. The difference from a true receive collision is that the switch from packet data to the jam pattern has already been made (controlled by /ANYXN). Thus the state of /COLN has no effect upon repeater operation. In common with the operation of the RECEIVE COLLISION state, the repeater remains in this condition until the collision and receive activity on PORT M subside. The packet repetition operation completes when the Tw1 recovery time in the WAIT state has been performed.

4.3.6.5 EXAMPLES OF PACKET REPETITION SCENARIOS

Jabber Protection

A repeater is required to disable transmit activity if the length of its current transmission reaches the jabber protect limit. This is defined by the IEEE specification's Tw3 time. The repeater disables output for a time period defined by the Tw4 specification, after this period normal operation may resume.

figure 13 shows the effect of a jabber length packet upon a LEMRIC based repeater system. The JABBER PROTECT state is entered from the SEND DATA state. While the Tw4 period is observed the Inter-LEMRIC bus displays the IDLE state. this is misleading since new packet activity or continuous activity (as shown in the diagram) does not result in packet repetition. This may only occur when the Tw4 requirement has been satisfied.



Note 1: The IEEE Specification does not have a jabber protect state defined in its main state diagram,this behavior is defined in an additional MAU Jabber Lock up Protection state diagram.

FIGURE 13. Jabber Protect

4.3.7 Port Block functions

The LEMRIC has 8 port logic blocks (one for each network connection). In addition to the packet repetition operations already described, the port block performs two other functions:

1. The physical connection to the network segment (transceiver function).
2. It provides a means to protect the network from malfunctioning segments (segment partition).

4.3.7.1 TRANSCEIVER FUNCTIONS

The LEMRIC may connect to network segments in two ways:

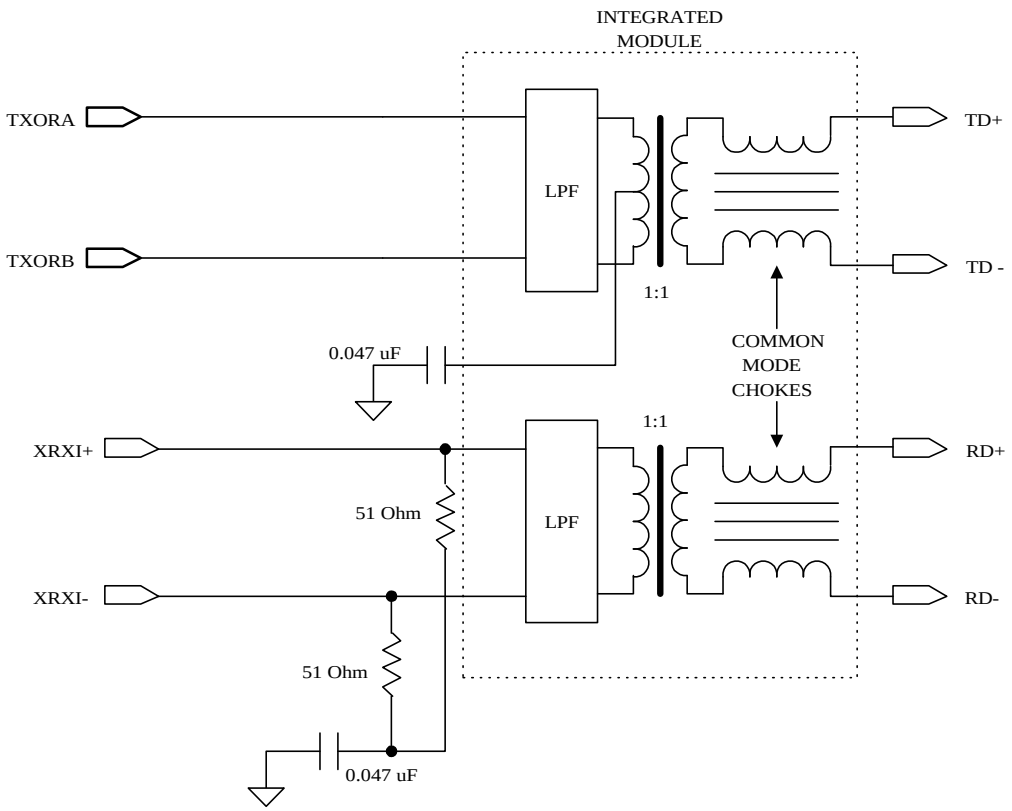
1. Over AUI cable to transceiver boxes (Port 1)
2. To twisted pair cable via a simple interface.

The first method is only supported by LEMRIC Port 1 (the AUI port). The other are available on Ports 2 to 9. The LEMRIC contains virtually all the digital and analog circuits required for connection to 10BASE-T network segments. The only optional additional active component is an external drive package. The connection for a LEMRIC port to a 10BASE-T segment is shown in figure 14. The diagram shows the components required to connect one of the LEMRIC's ports to a 10BASE-T segment (and lists a few module P/Ns and vendors). The major components is the integrated filter-transformer-choke module (or discrete combination of these functions).

The operation of the 10BASE-T transceiver's logical functions may be modified by hardware reset control. The default mode of operation is for the transceiver to transmit and expect reception of link pulses. This may be modified if the XTEST4 pin pulled down (pull down resistor is needed) before hardware reset operation. The port's transceiver will operate normally but will not transmit link pulses nor monitor their reception. Thus the entry to a link fail state and the associated modification of transceiver operation will not occur until another hardware reset and new logic setting on XTEST4 pin.

The on-chip 10BASE-T transceivers automatically detect and correct the polarity of the received data stream. This polarity detection scheme relies upon the polarity of the received link pulses and the end of packet waveform. Polarity detection and correction may be disable through XTEST3 pin pulled down by a resistor before hardware reset operation and the associated modification of transceiver operation will not occur until another hardware reset and new logic setting on XTEST3 pin.

when using external transceivers the user must perform collision detection and the other functions associated with an IEEE 802.3 Media Access Unit. figure 15 shows the connection between a repeater port and a coaxial transceiver using the AUI type interface.



Vendor	Filter-Transformer-Choke Modules
Pulse Engineering	PE65424,PE65434,PE65431
Bel Fuse	0556-2006-00,0556-2006-01
Valor	FL1010 (4 Channel),FL1012*,FL1020

* There is a single common mode choke on the transmit channel only.

FIGURE 14 . Port Connection to a 10BASE-T Segment and Some Typical Filter-Transformer-Choke Modules

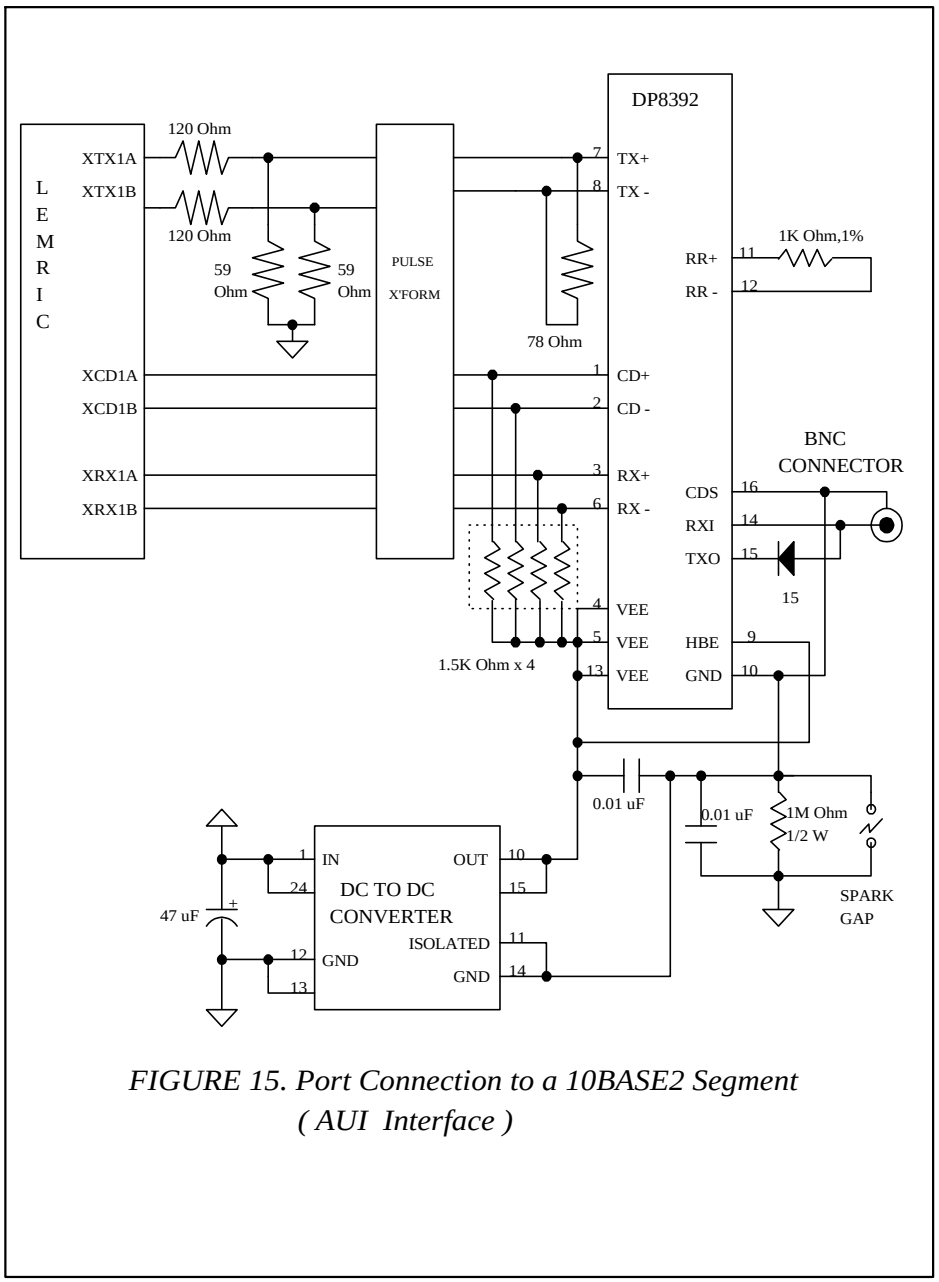


FIGURE 15. Port Connection to a 10BASE2 Segment
(AUI Interface)

5. Absolute Maximum Ratings

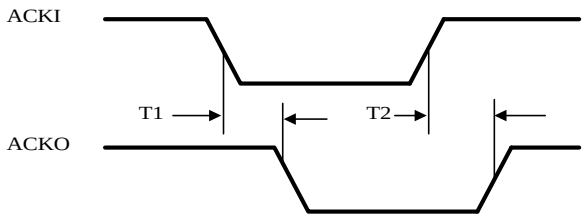
Supply Voltage (VCC)	4.75V	to	5.25V
DC Input voltage (VIN)	-0.5V	to	VCC+0.5V
DC Output Voltage (VOUT)	-0.5V	to	VCC+0.5V
Ambient Temperature Under Bias	0C	to	70C
Storage Temperature Range (TSTG)	-40C	to	125C
Operating Temperature Range	0C	to	70C
Power Dissipation (PD)	250mW	to	1150mW

6. D.C. Characteristics

Symbol	Description	Conditions	Min.	Max.	Units
VOH	Minimum High Level Output Voltage	IOH=-4mA	2.4	-	V
VOL	Minimum Low Level Output Voltage	IOL=8mA	-	0.4	V
VIH	Minimum High Level Input Voltage	VCC=5V	2.0	VCC	V
VIL	Maximum Low Level Input Voltage	VCC=5V	VSS	0.8	V
IIL	Input Low Current	VIN=1.0V	-	-0.5	uA
IIH	Input High current	VIN=VCC	-	20	uA
ICC	Supply current		-	230	mA
VDS	Differential Squelch Threshold (XRX1+-, XCD1+-)		+-190	+-280	mV
VRON	Minimum Receive Squelch Threshold (Twisted-Pair Port 2-9)		+-200	+-460	mV

7. Switching Characteristics

PORT ARBITRATION TIMING

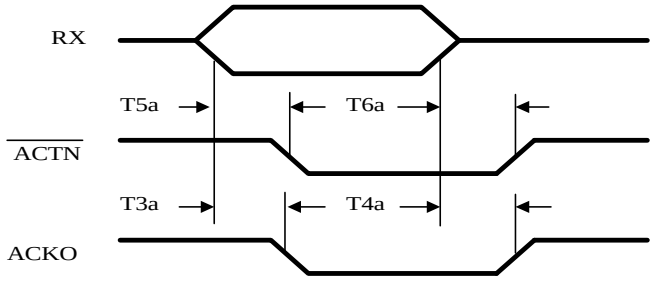


Symbol	Number	Parameter	Min	Max	Units
ackilackol	T1	ACKI Low to ACKO Low		220	ns
ackihackoh	T2	ACKI High to ACKO High		220	ns

Note : Timing valid with no receive or collision activities.

RECEIVE TIMING-AUI PORTS

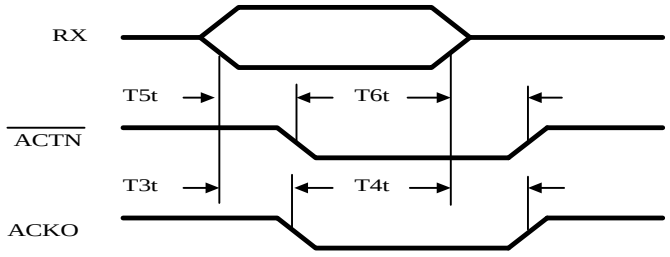
Receive activity propagation start up and end delays for ports in non 10BASE-T mode.



Symbol	Number	Parameter	Min	Max	Units
rxaackol	T3a	RX Active to ACKO Low	250	350	ns
rxiackoh	T4a	RX Inactive to ACKO High (Note 1)	1900	2000	ns
rxaactnl	T5a	RX Active to ACTN Low	250	350	ns
rxiactnh	T6a	RX Inactive to ACTN High (Note 1)	1960	2060	ns

Note : ACKI assumed high
Note 1 : This time includes EOP. & FIFO Data clear time.

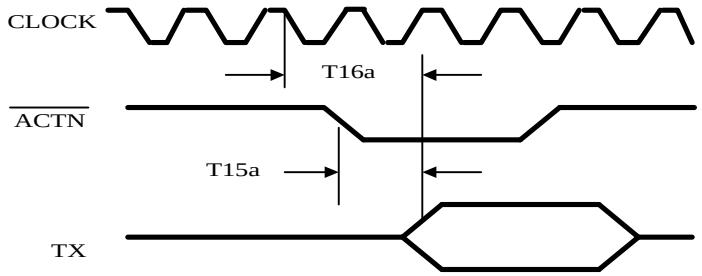
RECEIVE TIMING-10BASE-T PORTS
Receive activity propagation start up and end delays for ports in 10BASE-T mode



Symbol	Number	Parameter	Min	Max	Units
rxaackol	T3t	RX Active to ACKO Low	550	650	ns
rxiackoh	T4t	RX Inactive to ACKO High (Note 1)	1300	1400	ns
rxaactnl	T5t	RX Active to ACTN Low	550	650	ns
rxiactnh	T6t	RX Inactive to ACTN High (Note 1)	1360	1460	ns

Note : ACKI assumed high.
Note 1 : This time includes EOP. & FIFO Data clear time.

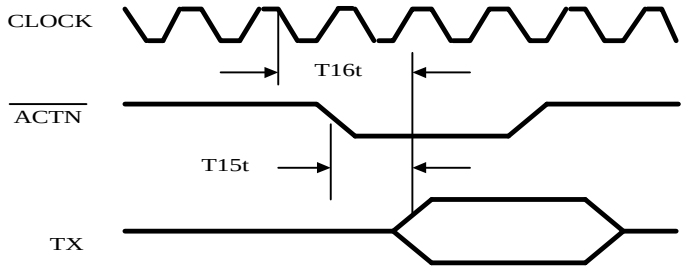
TRANSMIT TIMING-AUI PORTS
Transmit activity propagation start up and end delays for ports in non 10BASE-T mode



Symbol	Number	Parameter	Min	Max	Units
actnltxa	T15a	/ACTN Low to TX Active		260	ns
clkitxa	T16a	CLOCK in to TX Active (Note 1)		270	ns

Note : ACKI assumed high.
Note 1 : Clock not drawn to scale.

TRANSMIT TIMING-10BASE-T PORTS
Receive activity propagation start up and end delays for ports in 10BASE-T mode

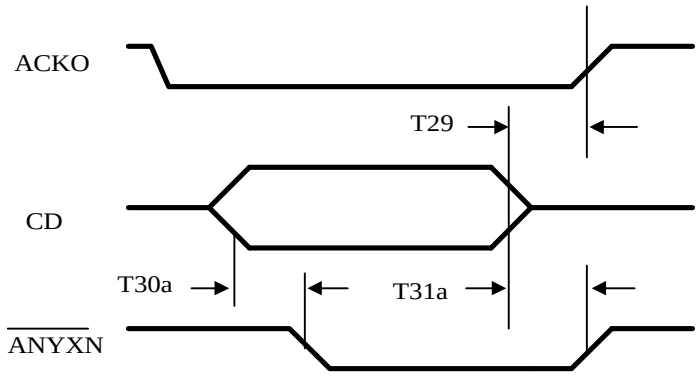


Symbol	Number	Parameter	Min	Max	Units
actnltxa	T15a	/ACTN Low to TX Active		260	ns
clkitxa	T16a	CLOCK in to TX Active (Note 1)		270	ns

Note : ACKI assumed high.
Note 1 : Clock not drawn to scale.

COLLISION TIMING-AUI PORTS
Collision activity propagation start up and end delays for ports in non 10BASE-T mode

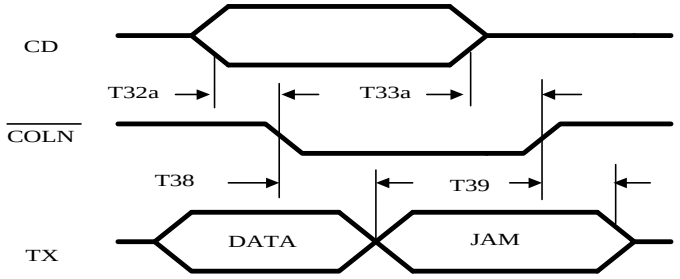
TRANSMIT COLLISION TIMING



Symbol	Number	Parameter	Min	Max	Units
cdiackoh	T29	CD Inactive to ACKO High	450	550	ns
cdaanyxnl	T30a	CD Active to ANYXN Low	100	200	ns
cdianyxnh	T31a	CD Inactive to ANYXN High (Notes 1,2)	510	610	ns

Note 1 : TX collision extension has already been performed and no other port is driving /ANYXN.
Note 2 : Includes TW2.

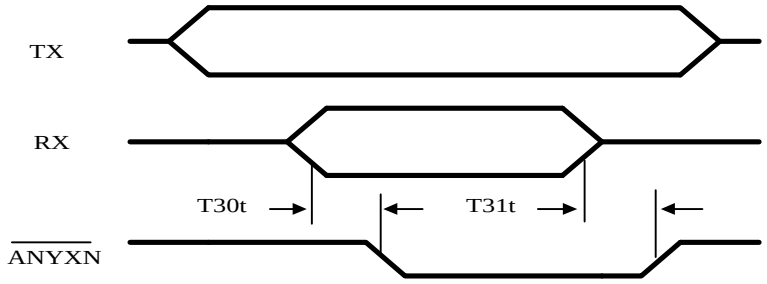
RECEIVE COLLISION TIMING



Symbol	Number	Parameter	Min	Max	Units
cdacoina	T32a	CD Active to /COLN Low	100	200	ns
cdicolni	T33a	CD Inactive to /COLN High	510	610	ns
colnljs	T38	/COLN Low to Start of JAM		300	ns
colnhje	T39	/COLN High to End of JAM (Note 1)		350	ns

Note 1: Reception ended before /COLN goes high.

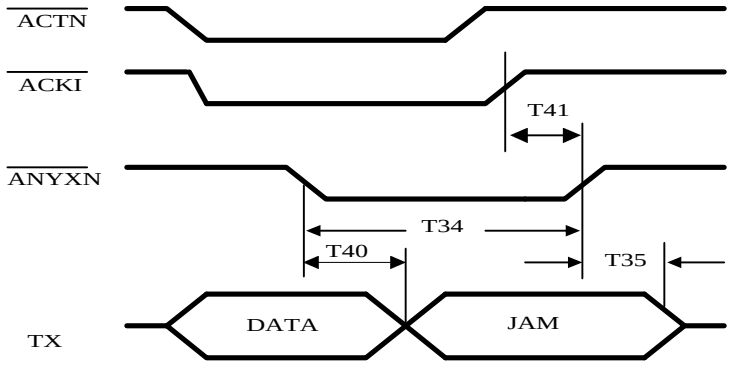
COLLISION TIMING-10BASE-T PORTS
Collision activity propagation start up and end delays for parts in 10BASE-T mode



Symbol	Number	Parameter	Min	Max	Units
colaanyl	T30t	Collision Active to /ANYXN Low	550	650	ns
colianyh	T31t	Collision inactive to /ANYXN High (Note 1)	360	460	ns

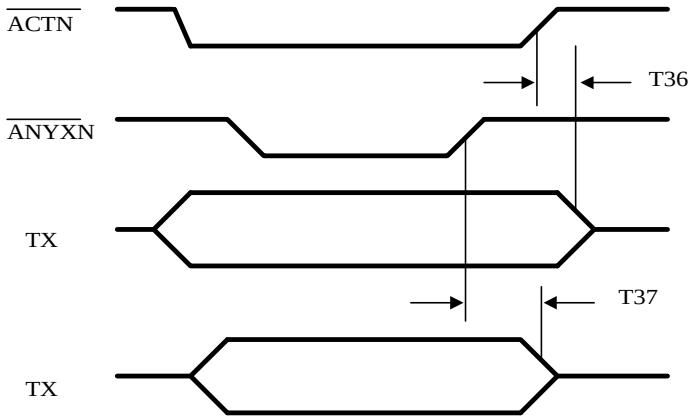
Note 1 : TX collision extension has already been performed and no other port is asserting /ANYXN.

COLLISION TIMING-ALL PORTS



Symbol	Number	Parameter	Min	Max	Units
T34	anylmin	/ANYXN Low Time	96		bits
T35	anyhtxai	/ANYXN High to TX to All Inactive		350	ns
T40	anylsj	/ANYXN Low to Start of JAM		300	ns
T41	ackihanyh	ACKI High to /ANYXN High		260	ns

COLLISION TIMING-ALL PORTS

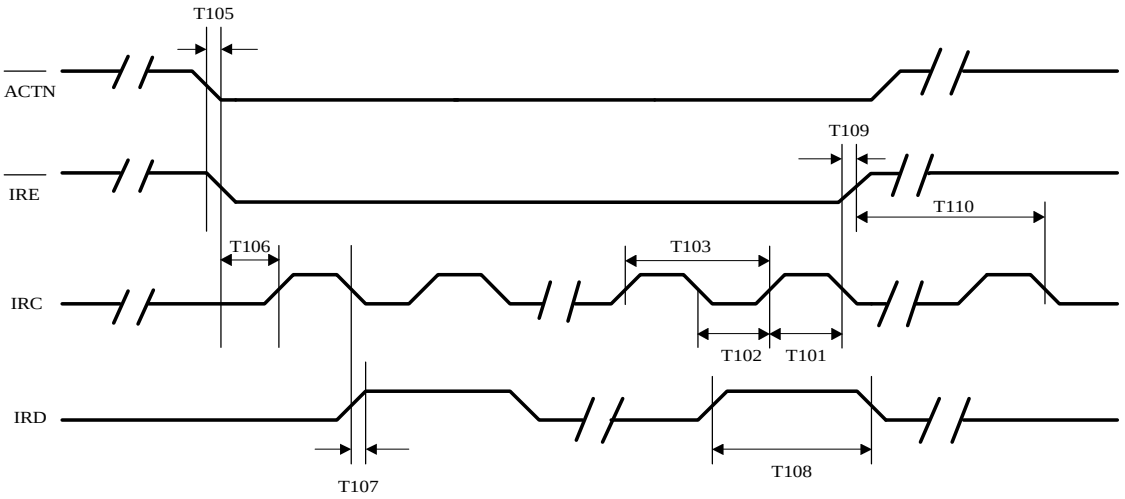


one port left

Symbol	Number	Parameter	Min	Max	Units
T36	actnntxi	/ACTN High to TX Inactive		150	ns
T37	anyhtxoi	/ANYXN High to TX "One Port Left" Inactive		200	ns

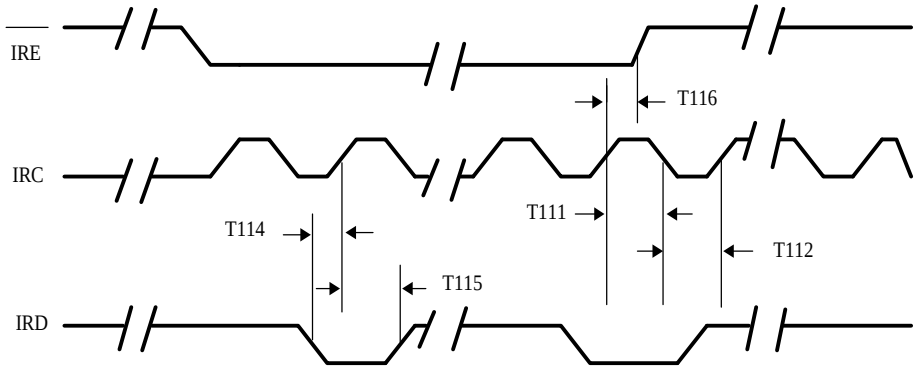
Note : 96 bits of JAM have already been propagated.

INTER-LEMRIC BUS OUTPUT TIMING



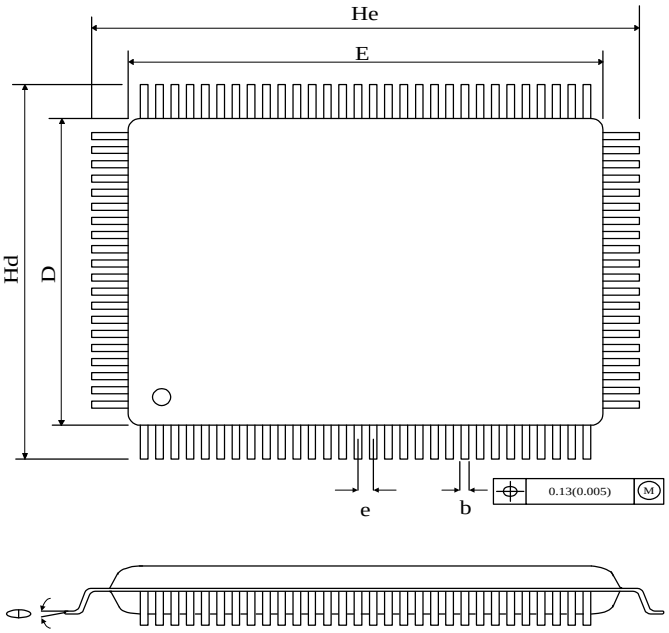
Symbol	Number	Parameter	Min	Max	Units
ircoh	T101	IRC Output High Time	40	60	ns
ircol	T102	IRC Output Low Time	40	60	ns
ircoc	T103	IRC Output Cycle Time	80	120	ns
actnolireol	T105	/ACTN Output Low to /IRE Output Low		10	ns
reolirca	T106	IRD Output Low to IRC Active		940	ns
irdov	T107	IRD Output valid from IRC		10	ns
irdos	T108	IRD Output Stable Valid Time	90		ns
ircohireh	T109	IRC Output High to /IRE High	50	65	ns
ircclks	T110	Number of IRCs after /IRE High	5	5	clocks

INTER-LEMRIC BUS INPUT TIMING



Symbol	Number	Parameter	Min	Max	Units
ircih	T111	IRC input High Time	30		ns
ircil	T112	IRC input Low Time	30		ns
irdisirc	T114	IRD input setup to IRC	10		ns
irdihirc	T115	IRD input Hold from IRC	10		ns
ircihireh	T116	IRC Input High to /IRC High	25	75	ns

8. Physical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.25	0.50	0.002	0.010	0.020
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e		0.65			0.0255	
Hd	18.75	19.00	19.25	0.783	0.748	0.758
He	24.75	25.00	25.25	0.984	0.984	0.994
L	1.05	1.20	1.35	0.047	0.047	0.053
L_1		2.50		0.041	0.098	
Y			0.08			0.003
θ	0		10	0		10

Note:For Exact Dimension,
Please use metric.
Inches are just approximation.

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