TC6097P

FAST ETHERNET REPEATER WITH PHY CONTROLLER

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FAST ETHERNET REPEATER WITH PHY CONTROLLER

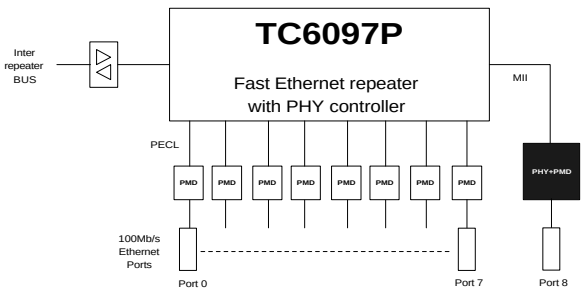
1. Features

- Functionally conforms to IEEE 802.3u. and meets IEEE Class II timing specification.
- Supports 9 network port (one for MII interface, others for TX PMD interface).
- Up to 31 repeater chips addressable for large hub cascadable application .
- One-chip elasticity buffer for PHY signal re-timing to the TC6097P clock source.
- Embedded LED output driver for per port (partition, receive) status, global jam status, RID error status, and global Traffic LED output driver.
- No external glue logic required.
- Separate jabber and partition state machines for each port.
- Supports PHY functions:
  - Link monitor function.
  - Carrier integrity monitoring (bypassable).
  - Stream cipher scrambler/descrambler (bypassable).
- 160 pin QFP.

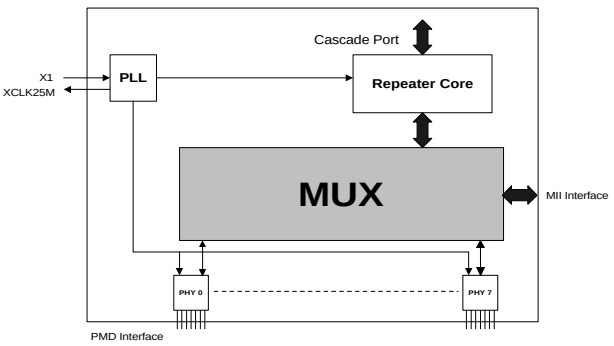
2. General Description

The TC6097P Fast Ethernet Repeater with PHY Controller contains a 100MHZ repeater core function and eight port PHY function in one chip. It can support eight TX PMD ports interface and one MII port. The TC6097P functions conform to IEEE 802.3u repeater unit specification.
The TC6097P directly supports 8 network connections. Larger repeaters may be constructed by cascading TC6097Ps together using the built in inter repeater bus.

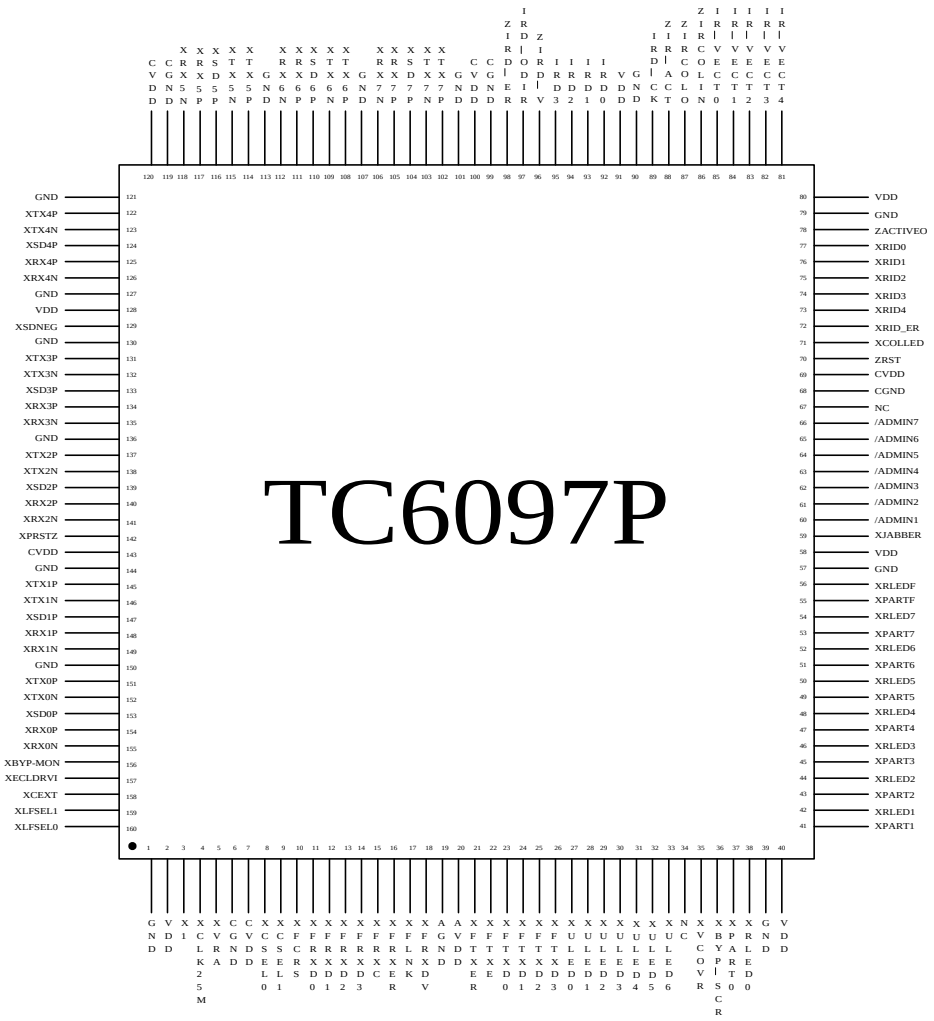
System Diagram



Block Diagram



3. Pin Connection Diagram



4. Pin Description

4.1 MII Interface To Phy (1 Of 3)

Signal Name	Type	Pin No	Description
XFRXD[3:0]	Ipu TTL	14,13,12,11	**RECEIVE DATA :** Nibble data inputs from each physical layer chip.
XFRXDV	Ipd TTL	18	**RECEIVE DATA VALID :** Asserted high when valid data is present on XFRXD[3:0].
XFRXER	Ipd TTL	16	**RECEIVE ERROR :** The physical layer asserts this signal high when it detects receive error.

4.1 MII Interface To Phy (2 of 3)

Signal Name	Type	Pin No	Description
XFRXC	Ipu TTL	15	**RECEIVE CLOCK :** Recovered clock from the physical layer device. XFRXD[3:0], XFRXDV, and XFRXER are generated from the falling edge of this clock.
XFCRS	Ipd TTL	10	**CARRIER SENSE :** Asynchronous carrier indication from the physical layer device.
XFTXE	O 8mA TTL	22	**TRANSMIT ENABLE :** Enable corresponding port for transmitting data.
XFTXER	O 8mA TTL	21	**TRANSMIT ERROR :** Asserted high when a code violation is requested to be transmitted.
XFTXD[0]	I/O Ipu 8mA TTL	23	**TRANSMIT DATA :** **Input function:** During Power Reset, This pin stay at low can set repeater core detect collision function base on data valid signal. **output function:** Nibble data output to be transmitted to physical layer device.
XFTXD[1]	I/O Ipu 8mA TTL	24	**TRANSMIT DATA :** **Input function:** During Power Reset, this pin stays at low can set the number of consecutive collisions limit of partition function to 128. Otherwise,The number is 64 . **output function:** Nibble data output to be transmitted to physical layer device.
XFTXD[2]	I/O Ipu 8mA TTL	25	**TRANSMIT DATA :** **Input function:** During Power Reset, this pin stays at low can make RXDV of port[7:0] replace CRS of port[7:0] to Repeater core and partition function deasserted by successful receive packet of each port. **output function:** Nibble data output to be transmitted to physical layer device.
XFTXD[3]	O 8mA TTL	26	**TRANSMIT DATA :** Nibble data output to be transmitted to physical layer device.
XFLNK	I/O Ipd 8mA TTL	17	**LINK OK INPUT :** If MII LINK OK Signal(High) input to this pin. XRLEDF will output Low to indicate MII port LINK OK.

4.2 Inter Repeater Bus Interface (1 of 2)

Signal Name	Type	Pin No	Description
IRD[3:0]	I/O Ipu 8mA TTL	95,94,93,92	**INTER REPEATER DATA :** Nibble data input/output. Transfers data from the active TC6097P to all other inactive TC6097Ps. The busmaster of the IRD bus is determined by IR_VECT bus arbitration.
ZIRD_V	I/O Ipu 8mA TTL	96	**INTER REPEATER DATA VALID :** This signal is used to frame good packets.

4.2 Inter Repeater Bus Interface (2 of 2)

Signal Name	Type	Pin No	Description
ZIRD_ER	I/O Ipu 8mA TTL	98	**INTER REPEATER DATA ERROR :** Used to track receive errors from the physical layer in real-time.
IRD_CK	I/O Ipu 8mA TTL	89	**INTER REPEATER DATA CLOCK :** All inter repeater signals are synchronized to the rising edge of this clock.
IRD_ODIR	O 8mA TTL	97	**INTER REPEATER DATA OUTWARD DIRECTION :** This pin indicates the direction of data for an external transceiver. It is high when IRD[3:0], ZIRD_V, ZIRD_ER, and IRD_CKare driven out towards the inter repeater bus, and low when data is being received from the bus.
ZACTIVEO	O 4mA CMOS	78	**ACTIVE OUT :** Enable for the IR_VECT[4:0] and ZIR_ACT signals.
IR_VECT[4:0]	I/O Ipu 8mA CMOS	81,82,83, 84,85	**INTER REPEATER VECTOR :** When the repeater senses at least one of its ports active, it drives its unique RID vector onto these pins. If the vector value read back differs from its own, this TC6097P will not drive the inter repeater signals and will de-assert its own vector value. If the value read back is the same as its own RID number this TC6097P will continue to drive the inter repeater bus signals.
ZIR_ACT	I/O Ipu 8mA CMOS	88	**INTER REPEATER ACTIVITY :** This output is asserted when the repeater senses network activity.
ZIRCOLO	O 8mA CMOS	87	**INTER REPEATER COLLISION OUT:** Asserted when the repeater sense network at collision state.
ZIRCOLIN	Ipu CMOS	86	**INTER REPEATER COLLISION IN :** Indicate from ZIRCOLO ,The repeater sense network at collision state.

4.3 TX -PMD Interface (1 of 2)

Signal Name	Type	Pin No	Description
XTX[0:7]P/N	O PECL	151,152, 145,146, 137,138, 131,132, 122,123, 114,115, 108,109, 102,103	**PECL DATA OUTPUT PORT:** 125Mb/s serialized differential PECL data transmit to PMD.
XSD[0:7]P	I PECL	153,147, 139,133, 124,116, 110,104	**SIGNAL DETECT INPUT:** PECL Signal from PMD indicating that received signal is above TP-PMD ANSI standard signal level.

4.3 TX -PMD Interface (2 of 2)

Signal Name	Type	Pin No	Description
XRX[0:7]P/N	I PECL	154,155, 148,149, 140,141, 134,135, 125,126, 117,118, 111,112, 105,106	**RECEIVED DATA INPUT :** NRZI PECL differential data from PMD.

4.4 Miscellaneous & Led Driver (1 of 2)

Signal Name	Type	Pin No	Description
X1	I CMOS	3	**LOCAL CLOCK :** Must be run at 25MHZ. Used for internal PLL clock reference.
XCLK25M	O CMOS	4	**CLOCK OUTPUT:** 25MHZ clock output from internal PLL .
XRID[4:0]	Ipd CMOS	73,74,75,7 6,77	**REPEATER IDENTIFICATION NUMBER :** Provides the unique vector for the IR_VECT[4:0] signals used in Inter Repeater bus arbitration.
ZRST	Ipd CMOS	70	**RESET :** This chip is reset when this signal is asserted low.
XPART[0:3]	I/O Ipu 8mA CMOS	37,41,43 ,45	**PARTITION LED (Active-Low) :** During power reset, This pin can be use to set internal test mode and must stay high for normal operation. After power Reset, these pins are active low to drive LEDs.Used to indicate each port partition status.
XPART[4:7]	O 8mA CMOS	47,49,51,5 3	**PARTITION LED (Active-Low) :** These pins are active low to drive LEDs. Used to indicate each port partition status.
XPARTF (/DISPART)	I/O Ipu 8mA CMOS	55	**PARTITION LED (Active-Low) :** Used to indicate MII port partition status. This status of XPARTF is latched into the DIS_PAR register (/DISPART) during power up/reset. 0 : Auto-Partition is disabled. 1 : Auto-Partition is not disabled.
XJABBER (/ADMIN[0])	I/O Ipu 8mA CMOS	59	**JABBER LED (Active-Low) :** This pin is active low to drive LEDs. Used to indicate any port jabber status. /ADMIN REGISTER : (/ADMIN[0]) At power-up/reset, the value on these pins are latched into /ADMIN REGISTER (/ADMIN[0]). Setting these bits to 1 enables the respective port (TX and RX). Latch a 0 to this bit will disable that port transmitting and receiving.
/ADMIN[1:7]	I/O Ipu 8mA CMOS	60,61, 62,63, 64,65, 66	**/ADMIN:** /ADMIN REGISTER : (/ADMIN[1:7]) At power-up/reset, the value on these pins are latched into /ADMIN REGISTER (/ADMIN[1:7]). Setting these bits to 1 enables the respective port (TX and RX). Latch a 0 to any bit will disable that port transmitting and receiving. Note: Latch a 0 into /ADMIN7, Disable port7 and MII port.

4.4 Miscellaneous & Led Driver (2 of 2)

Signal Name	Type	Pin No	Description
NC	O 8mA CMOS	67,34	**TMI internal TEST pin.**
XRLED0 XRLED[1:7]	O 8mA CMOS	38,42,44,46,48, 50,52,54	**RECEIVE LED (Active-Low) :** These pins are active low to drive LEDs. Used to indicate each port receive and link status.
XRLEDF	I/O Ipu 8mA CMOS	56	**RECEIVE LED (Active-Low) :** This pin used to indicate MII port Receive and Link states. It is active Low to drive LED.
XULED[0:6]	O 8mA CMOS	27,28,29,30,31, 32,33	**TRAFFIC LED (Active-low) :** These pins are active low to drive LEDs. Used to indicate traffic status.
XULED[0:6] to indicate Utilization as follow: XULED 0 1 2 3 4 5 6 UTILIZATION 1% 8% 32% 47% 63% 79% 95%			
XRID_ER	O 4mA CMOS	72	**REPEATER ID ERROR LED (Active-Low) :** This bit is set under two conditions : 1. When this TC6097P sees another TC6097P use the same RID number as its own on the Inter Repeater bus, or 2. XRID[4:0] has been programmed with a value of 1Fh. This bit sticks to Low until it is cleared (high) by a power-up/reset.
XCOLLED	O 8mA CMOS	71	**Collision LED (Active-Low) :** Used to indicate repeater collision status. This pin is active low to drive LED.
XBYP_MON	Ipd CMOS	156	Asserted high to bypass carrier Integrity function in port 7 to port 0.
XVCOVR	I	35	Analog PLL VCO delay time control pin.
XBYP_SCR	Ipd CMOS	36	Asserted high to bypass scrambler/descrambler function in port 7 to port 0.
XCSEL[0:1]	I/O Ipu 8mA CMOS	8,9	Test pin for internal use.
XLFSEL[0:1]	Ipd CMOS	160,159	test pin for internal use.
XSDNEG	I	129	Must bias at VCC-1.3V.
XECLDRVI	I	157	Current reference for PECL driver output .
XCEXT	I	158	Filter input for PLL.
XVRA	I	5	Current reference for PLL.
XPRSTZ	I	142	Analog PLL is Reset when this signal is asserted low. This input low period must be shorter the low period at ZRST pin. It means that the first is to release Analog PLL Reset signal and then to release Digital circuit Reset signal.

4.5 Power & Ground Pins

Signal Name	Type	Pin No	Description
VDD	P	2,40,58, 80,91, 128	Power pins for TC6097P I/O cell
GND	P	1,39,57, 79,90, 101,107, 113,121, 127,130, 136,144, 150	Ground pins for TC6097P I/O cell
CVDD	P	7,69, 100,120,14 3	Power pins for TC6097P core cell
CGND	P	6,68, 99,119	Ground pins for TC6097P core cell
AVDD	P	20	Power pins for TC6097P analog cell
AGND	P	19	Ground pins for TC6097P analog cell

4.6 Pin Type Designation

Pin Type	Description
Ipd (Ipu)	Input buffer and internal pull down. (pull up)
O	Output buffer, driven high or low at all times.
I/O Ipu	Bidirectional buffer with pull up.
I	Analogal input buffer.

5. Functional Description

The following sections describe the different functional blocks of TC6097P Fast Ethernet Repeater with PHY Controller.

5.1 Repeater State Machine

The Repeater State Machine (RSM) is the main block that governs the overall operation of the repeater. At any one time, the RSM is in one of the following four states : Idle, Repeat, Collision, or One Port Left.

5.1.1 Idle State

The RSM enters this state after reset or when there is no activity on the network and carrier sense is not present. The RSM exits this state if the above conditions are no longer true.

5.1.2 Repeat State

This state is entered when there is a reception on only one of the ports, port N. While in this state, the data is transmitted to all the ports but the reception port (port N). The RSM returns to Idle State when the reception ends, or transits to collision state if there are receiving activities on more than one port.

5.1.3 Collision State

When there are receiving activities on more than one port of the repeater, the RSM moves to Collision State. In this state, transmit data is replaced by Jam and sent out to all ports including the original port N. There are two ways for the repeater to leave the Collision State. The first is when there is no receiving activity on any of the ports. In this case the repeater moves to Idle State. The second is when there is only one port experiencing collision in which case the repeater enters the One Port Left State.

5.1.4 One Port Left State

This state is entered only from the Collision State.
While in this state, Jam is sent out to all ports except the port that has the receive activity. If more receiving activities occurs on any other port, then the repeater moves to Collision State, otherwise it will transit to Idle State when the receiving activity ends.

5.2 Port Control

When only one port has a receiving activity, the internal RXE signal (receive enable) is activated. If multiple ports are active, i.e. a collision scenario, then RXE will not be enabled for any port. The Port Select Logic asserts the outputs /IRCOLO and /IR_ACT to indicate to other cascaded TC6097Ps that there is collision or receiving activity present on this TC6097P.

5.3 TXE Control

This control logic enables the appropriate ports for data transmission according to the four states of the RSM.
That is, during Idle State, no ports are enabled ; during Repeat State, all ports but port N are enabled ; in Collision State, all ports including port N are enabled ; during One Port Left State all ports except the port experiencing the collision, will be enabled.

5.4 Data Path

After the port selection logic has enabled the active port, receive data (RXD), receive clock (RXC), receive error (RXER) and receive data valid (RXDV) will flow through the chip from that port out onto the Inter Repeater (IR) bus if no collisions are present. The signals on the IR bus flow either in to or out of the chip depending upon the Repeater state.
If the TC6097P is currently receiving and no collisions are present, the IR bus signals flow out of the chip. The TC6097P Arbitration Logic guarantees that only one TC6097P will gain ownership of the IR bus. In all other states, the IR signals are inputs.
When IR signals are inputs, the signals flow into the Elasticity Buffer (EB). Here, the data is re-timed and then sent out to the transmit ports. The Transmit Control logic determines which ports are enabled.
If a collision occurs, a Jam pattern is sent out from the EB instead of the data. Jam pattern (3,4,3,4,.....from the TC6097P, encoded by the Physical Layer device as 1,0,1,0,.....) is transmitted for the duration of the collision activity.

5.5 Jabber Protection State Machine

The jabber specification for 100BASE-T is functionally different from 10BASE-T. In 100BASE-T, when a port jabbers, its receive and transmit ports are cutoff until the jabber activity ceases. All other ports remain unaffected and continue normal operation. The jabber protect limit (i.e. the time for which a port can jabber until it is cutoff) for the TC6097P is 60K bit times.

5.6 Auto-Partition State Machine

In order to protect the network from a port that is experiencing excessive consecutive collisions, each port has its own auto-partition state machine.

A port with excessive consecutive collisions will be partitioned after 64 consecutive collisions occur on that port. Transmitting ports will not be affected.

A partitioned port will be reconnected when a collision-free packet of length 64Bytes or more is received from other port.

The TC6097P also provides a configuration bit that disables the auto-partition function completely.

5.7 Inter Repeater Bus Interface

The lnter Repeater bus is used to connect multiple TC6097Ps together to form a logical repeater unit and also to allow a managed entity. The IR bus allows received data packets to be transferred from the receiving TC6097P to the other TC6097Ps in the system. These TC6097Ps then send the data stream to their transmit enabled ports.

Notification of collisions to other cascaded TC6097Ps is as important as data transfer across the network. The IR bus has a set of status lines capable of conveying collision information between TC6097Ps to ensure their main state machines operate in the appropriate manner.

The IR bus consists of the following signals :

- Inter Repeater Data. This is the transfer data, in nibble format, from the active TC6097P to all other cascaded TC6097Ps.
- Inter Repeater Data Error. This signal carries the receive error status from the physical layer in real-time.
- Inter Repeater Data Valid. This signal is used to frame good packets.
- Inter Repeater Data Clock. All IR data is synchronized to this clock.
- Inter Repeater Data Outward Direction. This pin indicates the direction of the data flow with respect to the TC6097P. When the TC6097P is driving the IR bus (i.e. it contains port N) this signal is HIGH and when the TC6097P is receiving data from other TC6097Ps over the IR bus this signal is LOW.
- Inter Repeater Activity. When there is network activity the TC6097P asserts this output signal.
- Inter Repeater Collision Output. If there are multiple receptions on ports of a TC6097P or if the TC6097P senses a concurrent activity on another TC6097P it asserts this output.
- Inter Repeater Collision Input. This input indicates that one of the cascaded TC6097Ps is experiencing a collision.
- Inter Repeater Vector. When there is reception on a port the TC6097P drives a unique vector onto these lines. The vector on the IR bus is compared with the Repeater ID (RID). The TC6097P will continue to drive the IR bus if both the vector and RID match.
- Active Output. This signal is asserted by a TC6097P when at least one of its ports is active. It is used to enable external bus transceivers.

6. Absolute Maximum Ratings

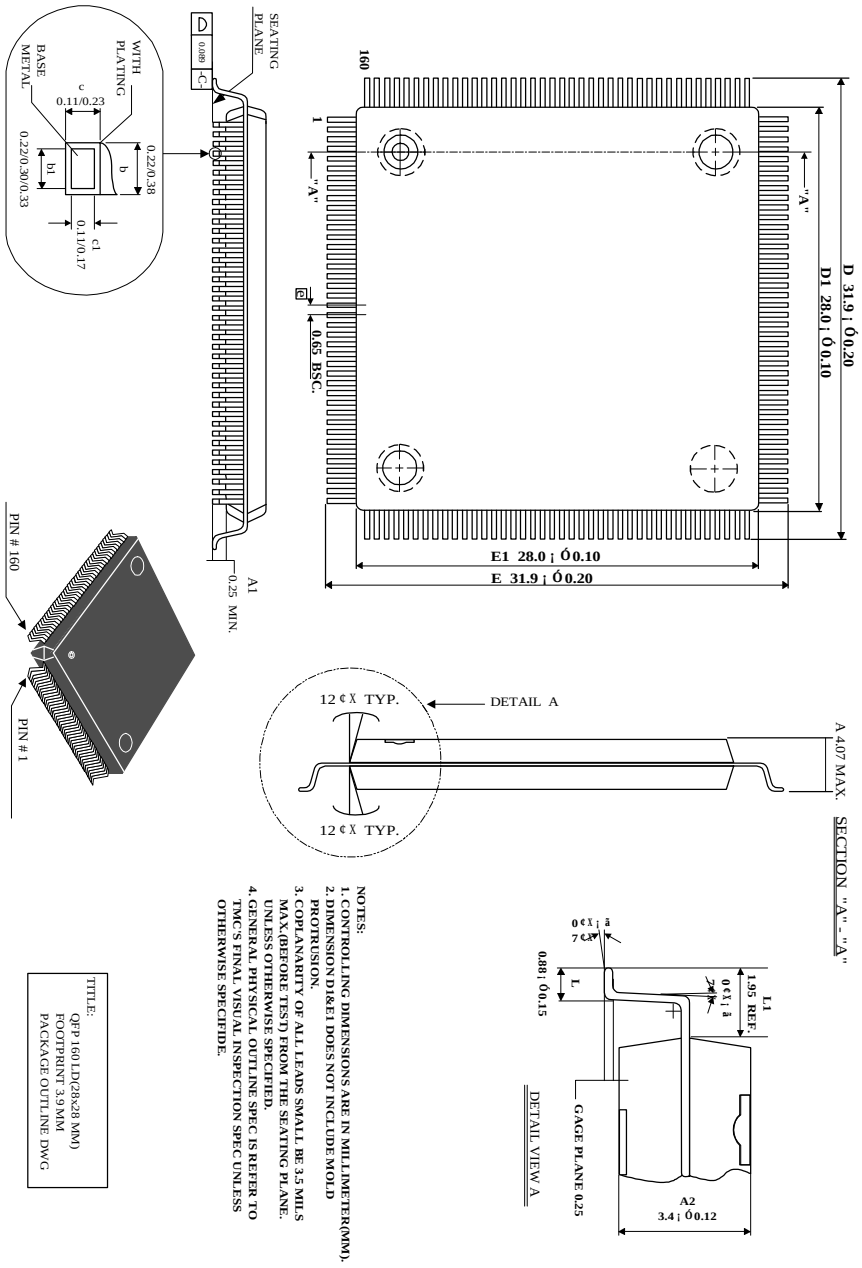
Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC	-0.3	6	V
Operations Temperature	Top	0	70	℃
Storage Temperature	TSt	-65	150	℃

7. DC Specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Minimum High Level Input Voltage	TTL Input CMOS Input PECL Input	2.0 0.7xVCC VCC-1.16		V
V_{IL}	Maximum Low Level Input Voltage	TTL Input CMOS Input PECL Input		0.8 0.3xVCC VCC-1.47	V
V_{OH}	Minimum High Level Output Voltage	I_{OH} = -4 mA TTL Output CMOS Output PECL Output (Note 1)	 3.7 0.9xVCC VCC-1.02		V
V_{OL}	Maximum Low Level Output Voltage	I_{OL} = 1 to 4 mA TTL Output CMOS Output PECL Output (Note 1)		 0.5 0.1xVCC VCC-1.62	V
I_{IN}	Input Current	With Internal Pullup		±150	µA
		Without Internal Pullup		±10	
I_{OZ}	TRI-STATE Output Leakage Current	With Internal Pullup		±150	µA
		Without Internal Pullup		±10	
I_{CC}	Operating Current	Typical V_{CC} = 5V		TBD	mA

Note 1: Without external load

8. Physical Dimensions (160pin QFP)



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