4.1.2 J6: LVDS Connector

Pin #	Signal Name	Function
1	TXO3M	Negative LVDS differential data input. Channel O3 (odd)
2	TXO3P	Positive LVDS differential data input. Channel O3 (odd)
3	TXOCKM	Negative LVDS differential clock input. (odd)
4	TXOCKP	Positive LVDS differential clock input. (odd)
5	TXO1M	Negative LVDS differential data input. Channel O1 (odd)
6	TXO2P	Positive LVDS differential data input. Channel O1 (odd)
7	TXO1M	Negative LVDS differential data input. Channel O1 (odd)
8	TXO1P	Positive LVDS differential data input. Channel O1 (odd)
9	TXO0M	Negative LVDS differential data input. Channel O0 (odd)
10	TXO0P	Positive LVDS differential data input. Channel O0 (odd)
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	TXE3P	Positive LVDS differential data input. Channel E3 (even)
18	TXE3M	Negative LVDS differential data input. Channel E3 (even)
19	TXECKP	Positive LVDS differential data input. (even)
20	TXECKM	Negative LVDS differential data input. (even)
21	TXE2P	Positive LVDS differential data input. Channel E2(even)
22	TXE2M	Negative LVDS differential data input. Channel E2(even)
23	TXE1P	Positive LVDS differential data input. Channel E1(even)
24	TXE1M	Negative LVDS differential data input. Channel E1(even)
25	TXE0P	Positive LVDS differential data input. Channel E0(even)
26	TXE0M	Negative LVDS differential data input. Channel E0(even)
27	LCD VCC	+5.0V power supply
28	LCD VCC	+5.0V power supply
29	LCD VCC	+5.0V power supply
30	LCD VCC	+5.0V power supply
31	GND	Ground
32	GND	Ground

4.1.3 J1: Inverter Connector

Pin #	Signal Name	Function
1	VIN	+19V
2	VIN	+19V
3	GND	Ground
4	GND	Ground
5	On/Off control	On/Off Control
6	GND	Ground
7	Brightness	Brightness control Vadj = 5V~0V

4.1.4 J2 Power

Pin #	Signal Name	Function
1	+12V	+12V Power Input
2	GND	Ground

4.1.5 W1: D-SUB

Pin #	Signal Name	Function
1	R_{IN}	Red Video
2	G_{IN}	Green Video
3	BIN	Blue Video
4	GND	Ground
5	GND	Ground
6	R_{RET}	Red Video Ground
7	G_{RET}	Green Video Ground
8	B_{RET}	Blue Video Ground
9	DCCVCCC	DDCVCC
10	GND	Ground
11	GND	Ground
12	V SDA	V SDA
13	HSYIN	H-Sync
14	VSYIN	V-Sync
15	V SCL	Clock Line (SCL)

4.1.6 J9 Switch Board Connector

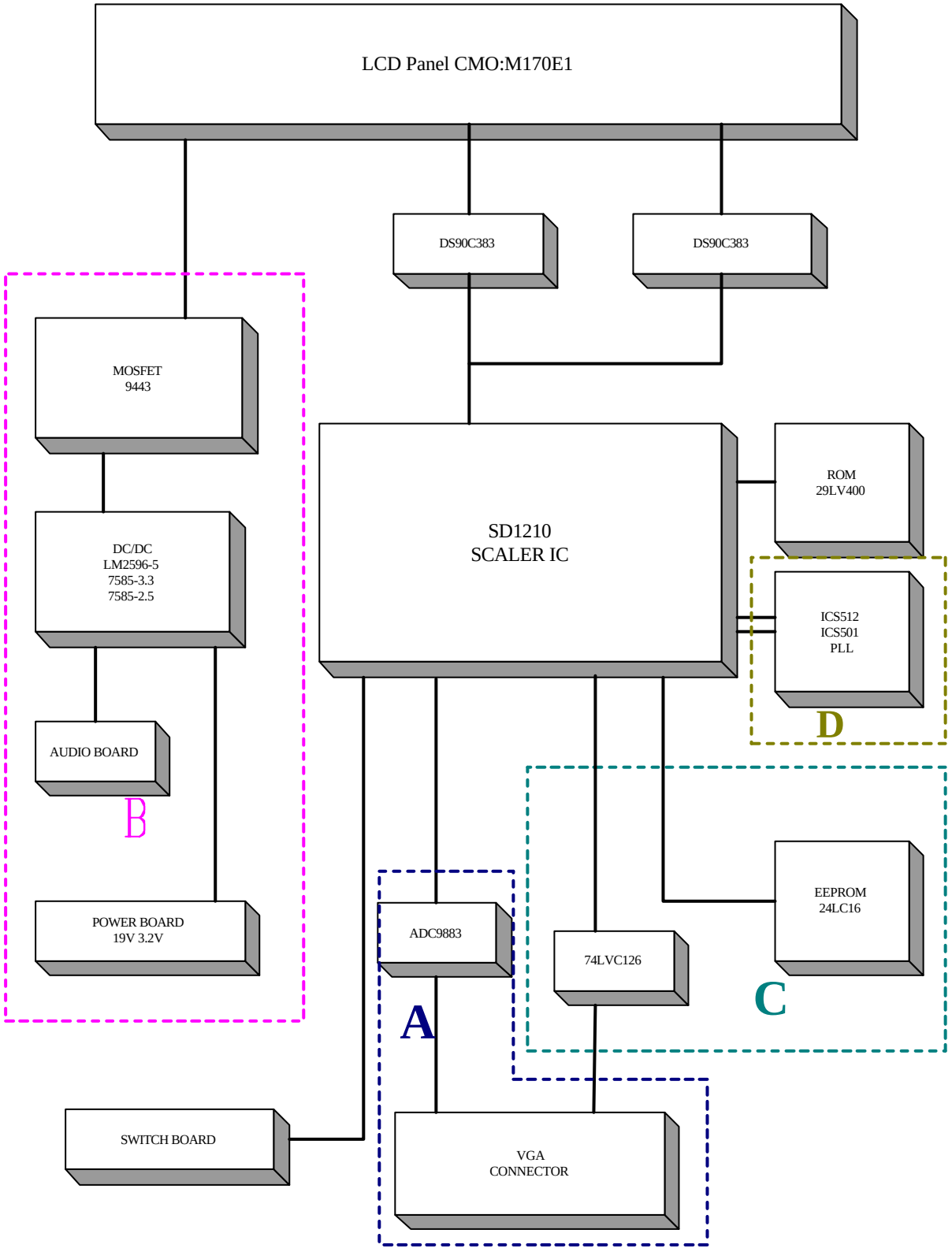
Pin #	Signal Name	Function
1	GND	GROUND
2	+5V	+5V POWRE SUPPLY
3	ON/OFF	ON/OFF
4	SUB	SUBTRACTION Key
5	ADD	ADDITION Key
6	DOWN	DOWN Key
7	NC	NO CONNECT
8	SELECT	SELECT KEY
9	OSD	OSD KEY
10	LED GRN	LED GREEN
11	LED ORG	LED ORANGE (AMBER)
12	LED MUTE	LED MUTE

4.1.7 J11: Audio Board Connector

Pin #	Signal Name	Function
1	+5V	+5V POWRE SUPPLY
2	GND	GROUND
3	VOLUME	VOLUME CONTROL

SECTION 6 THEORY OF OPERATION

6.1 System Block Diagram



6.2 System Circuitry Description

BLOCK A.

In reference of the block diagram of the monitor's circuitry shown on the previous page, the analog RGB inputs are amplified and sent through an analog-to-digital converter (ADC) to a digital signal processor (DSP) that generates digital RGB signals for controlling LCA panel.

BLOCK B.

A second power supply converts a single 19V supply to the various voltages needed to run the LCD panel and the inverter driving the display's backlights.

BLOCK C.

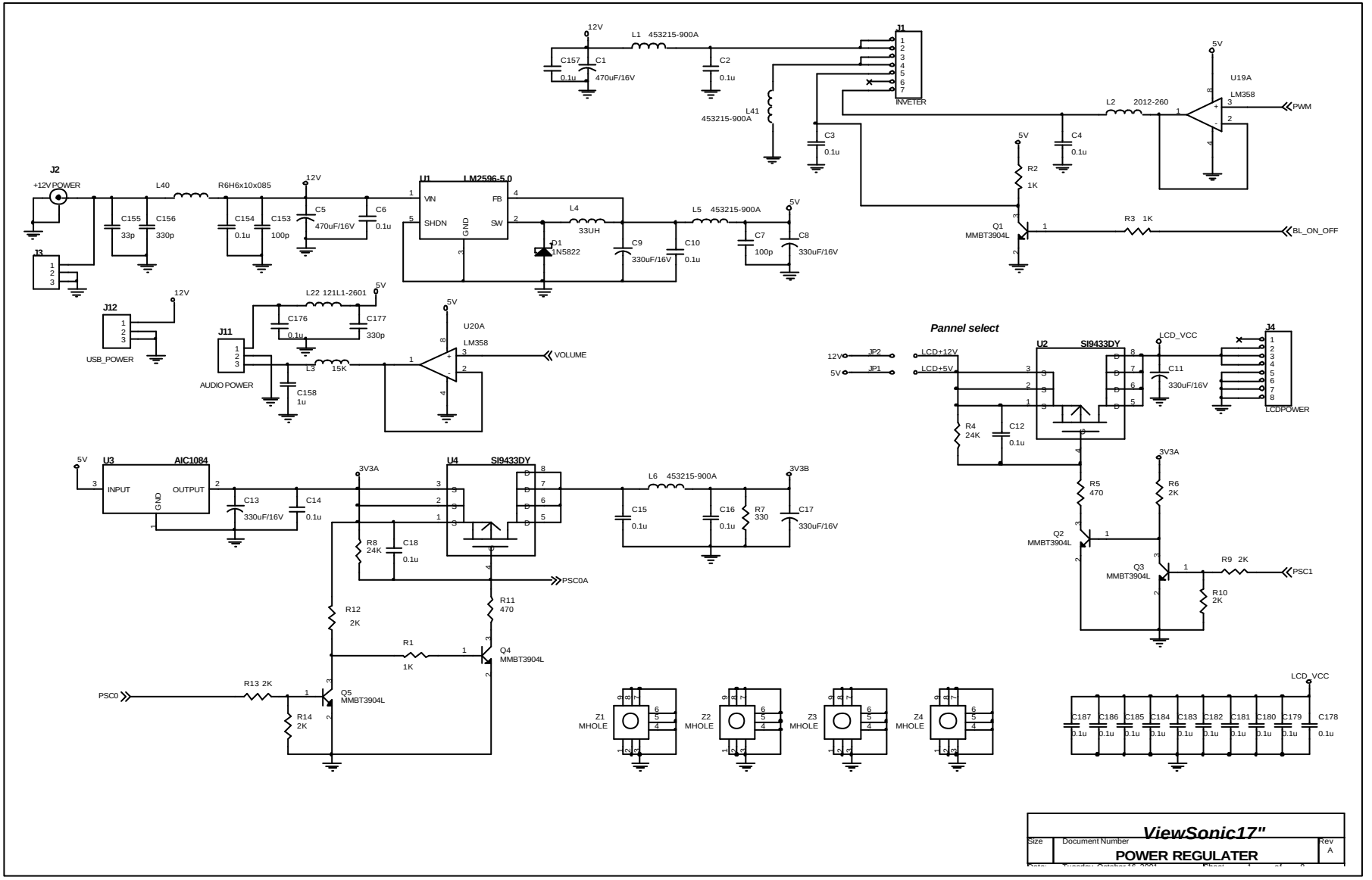
SYNC SIGNAL PROCESSOR. This processor determines the polarity of the horizontal and vertical sync signals, generates a fixed-polarity synchronized clock signal and provides data for use by the microprocessor in selecting circuit control parameters from EEPROM tables.

BLOCK D.

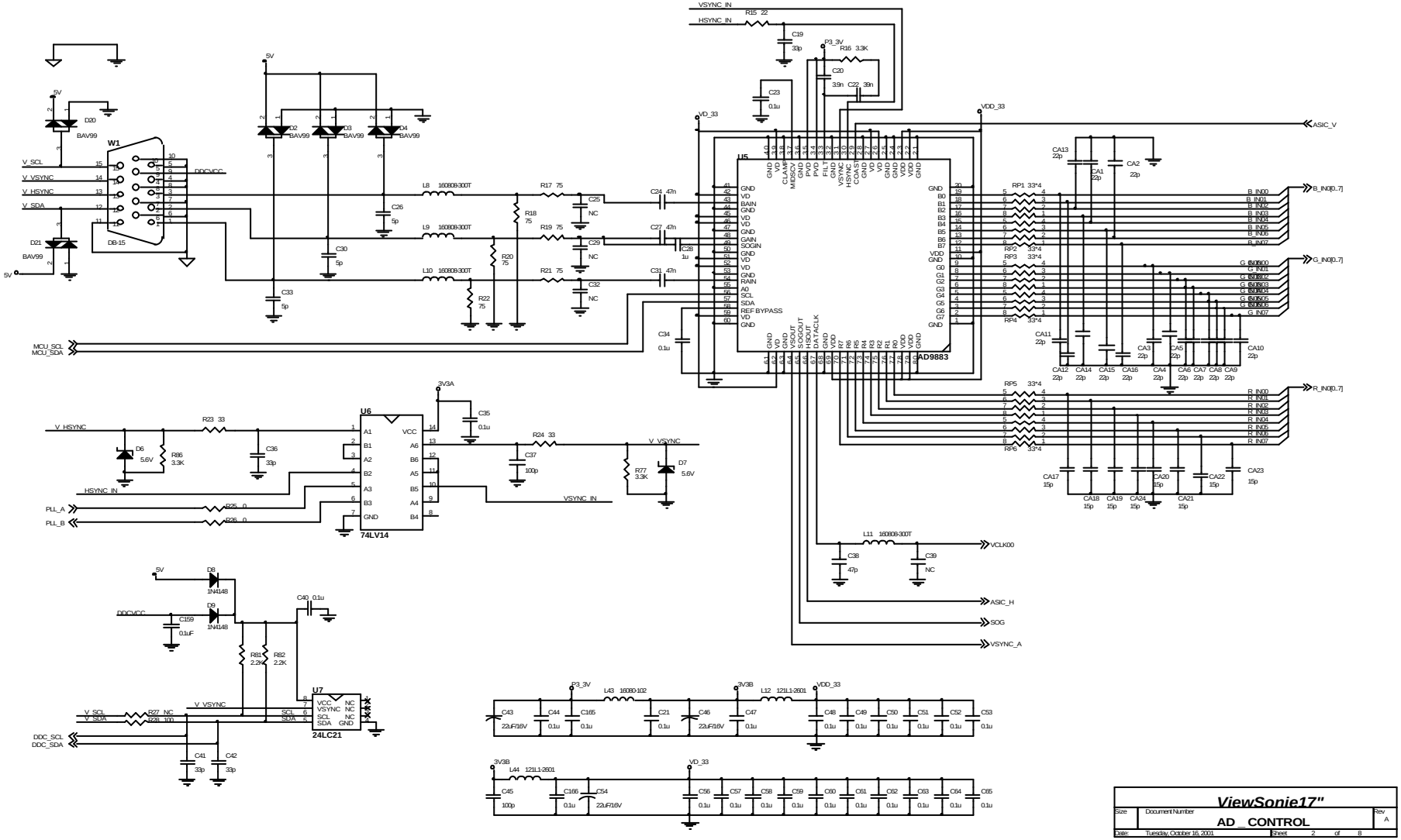
PLL CONTROLLER. The ADC digitizes the analog input in step with a trigger signal. The trigger signal must be synchronized to the personal computer's horizontal dot clock or screen noise will appear. While a phase-locked loop (PLL) reliably determines the correct frequency, manual adjustment available via the on-screen display enables the user to compensate for the phase differences occasionally seen among computer video adapters.

SECTION 9 CIRCUIT DIAGRAMS

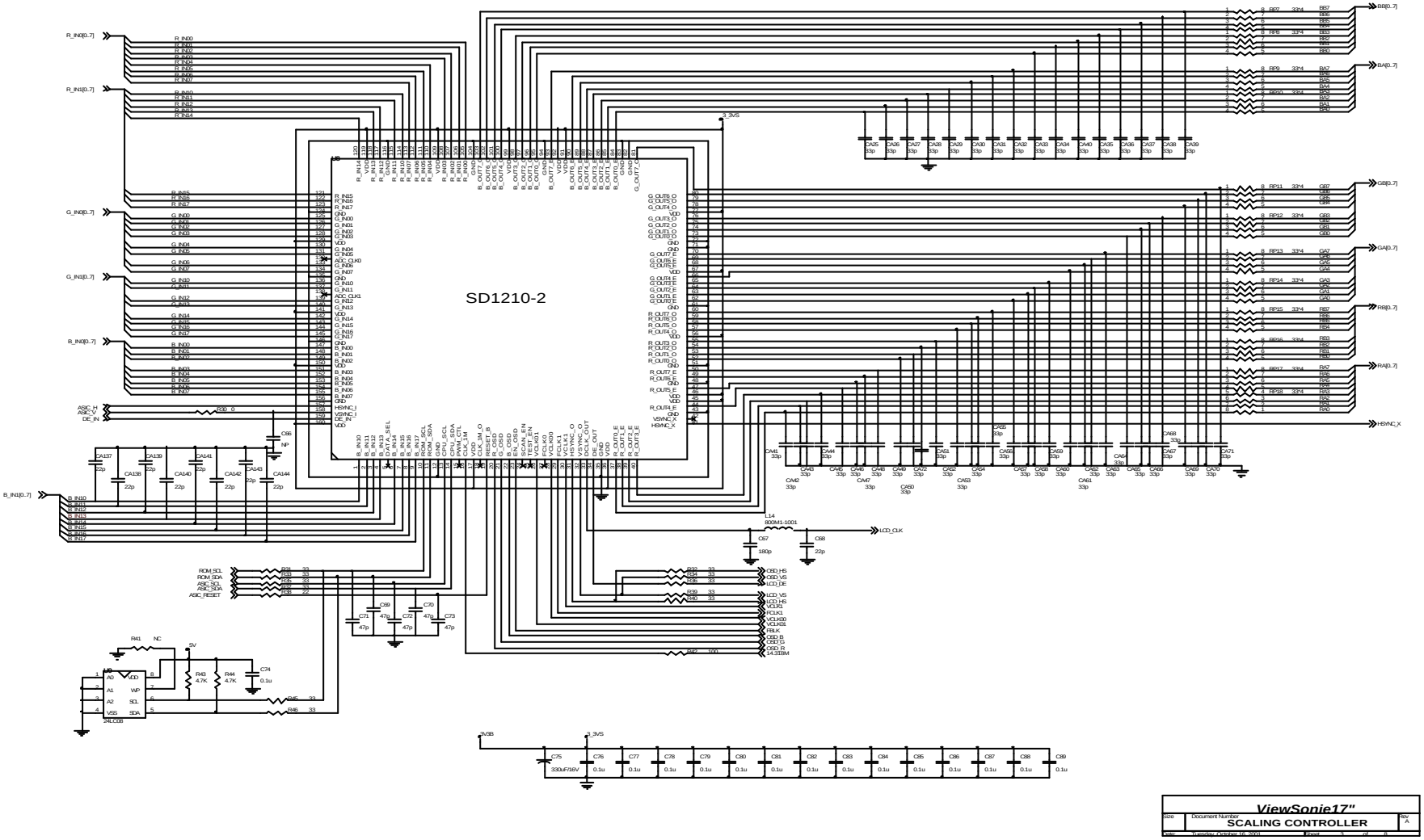
9.1 Power Regulator



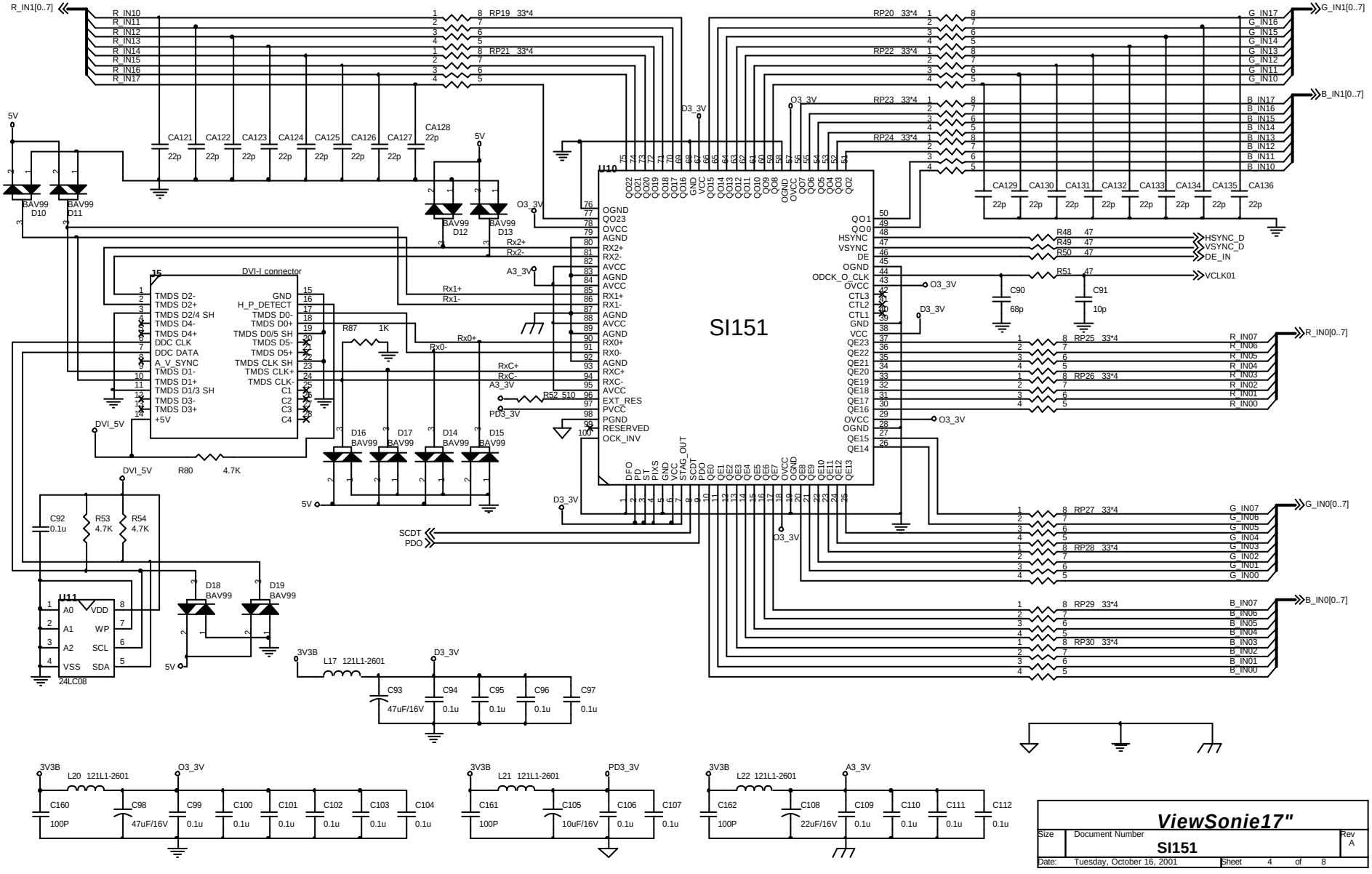
9.2 ADC


W1
D8-15
U5
AD9883
U6
74LV14
U7
24LC21
ViewSonic17"
AD_CONTROL
Tuesday, October 16, 2001
Sheet 2 of 8

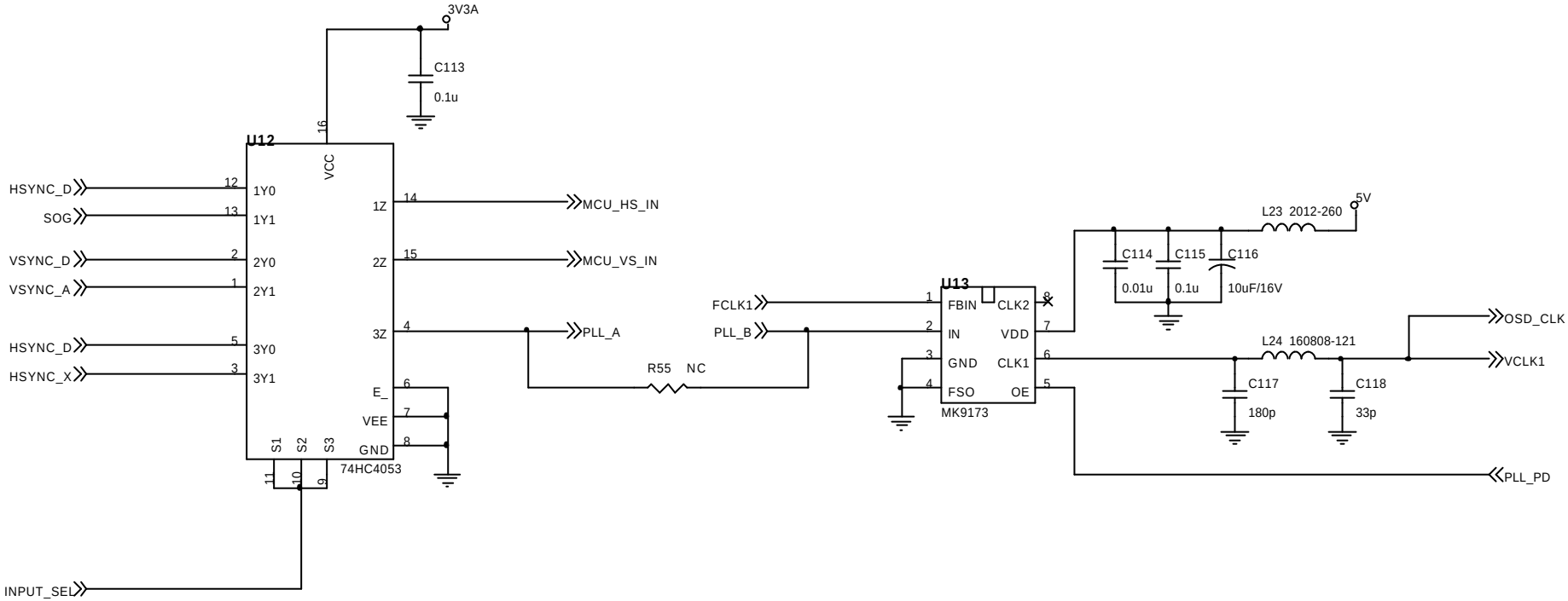
9.3 Scaling Controller



9.4 SI151

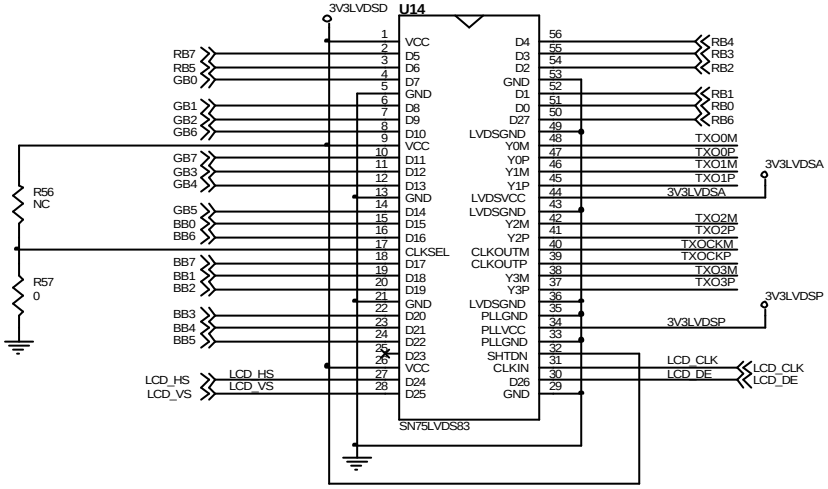

SI151
U10
J5
DVI-I connector
U11
24LC08
ViewSonie17"
SI151
Size
Document Number
Rev
A
Date: Tuesday, October 16, 2001
Sheet 4 of 8

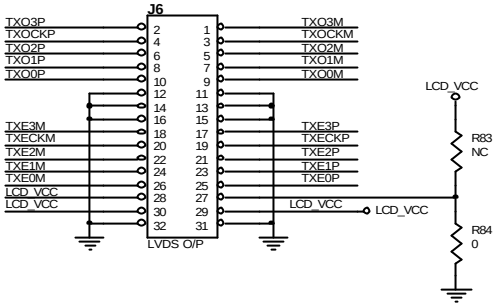
9.5 PLL

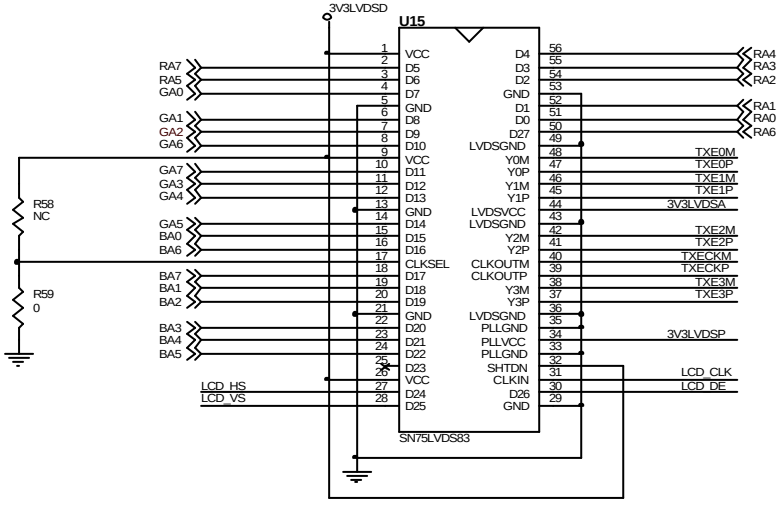


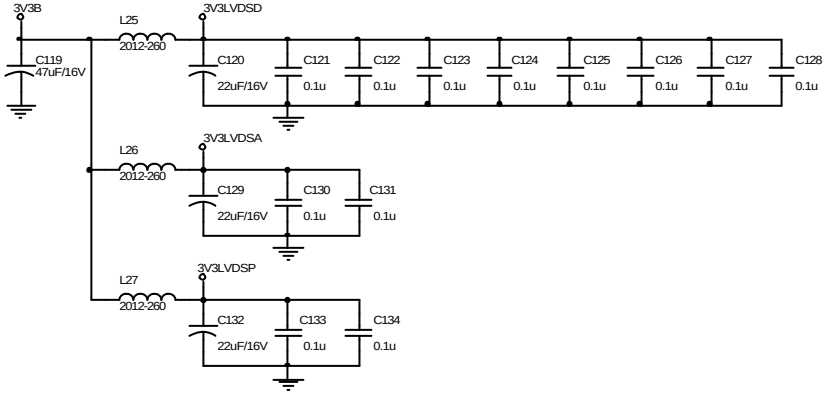
ViewSonic17"		
Size	Document Number: PLL	Rev: A
Date: Tuesday, October 16, 2001	Sheet 5 of 8	

9.6 LVDS



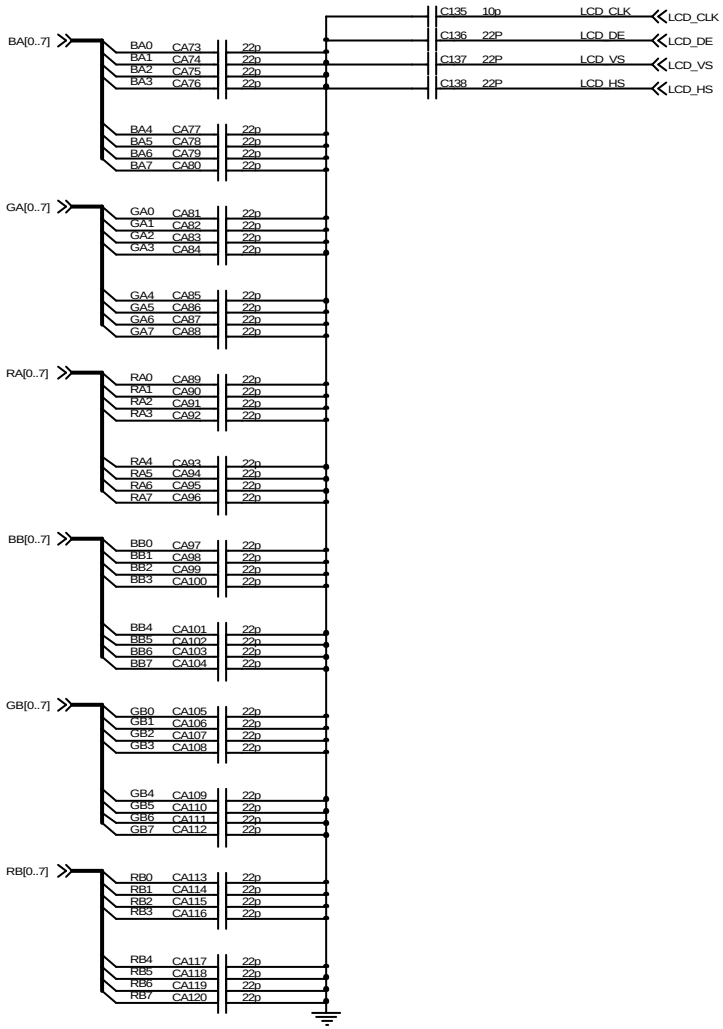


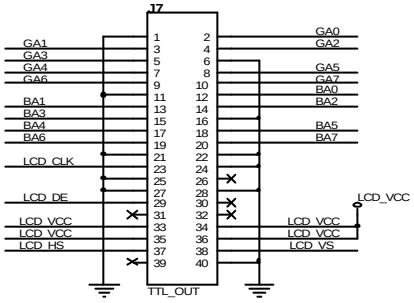


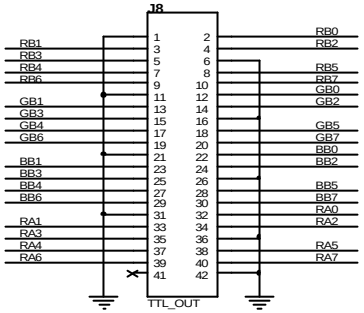


	ViewSonic17"		
Size	Document Number **LVDS**		Rev A
Date: Tuesday, October 16, 2001		Sheet 6 of 8	

9.7 TTL

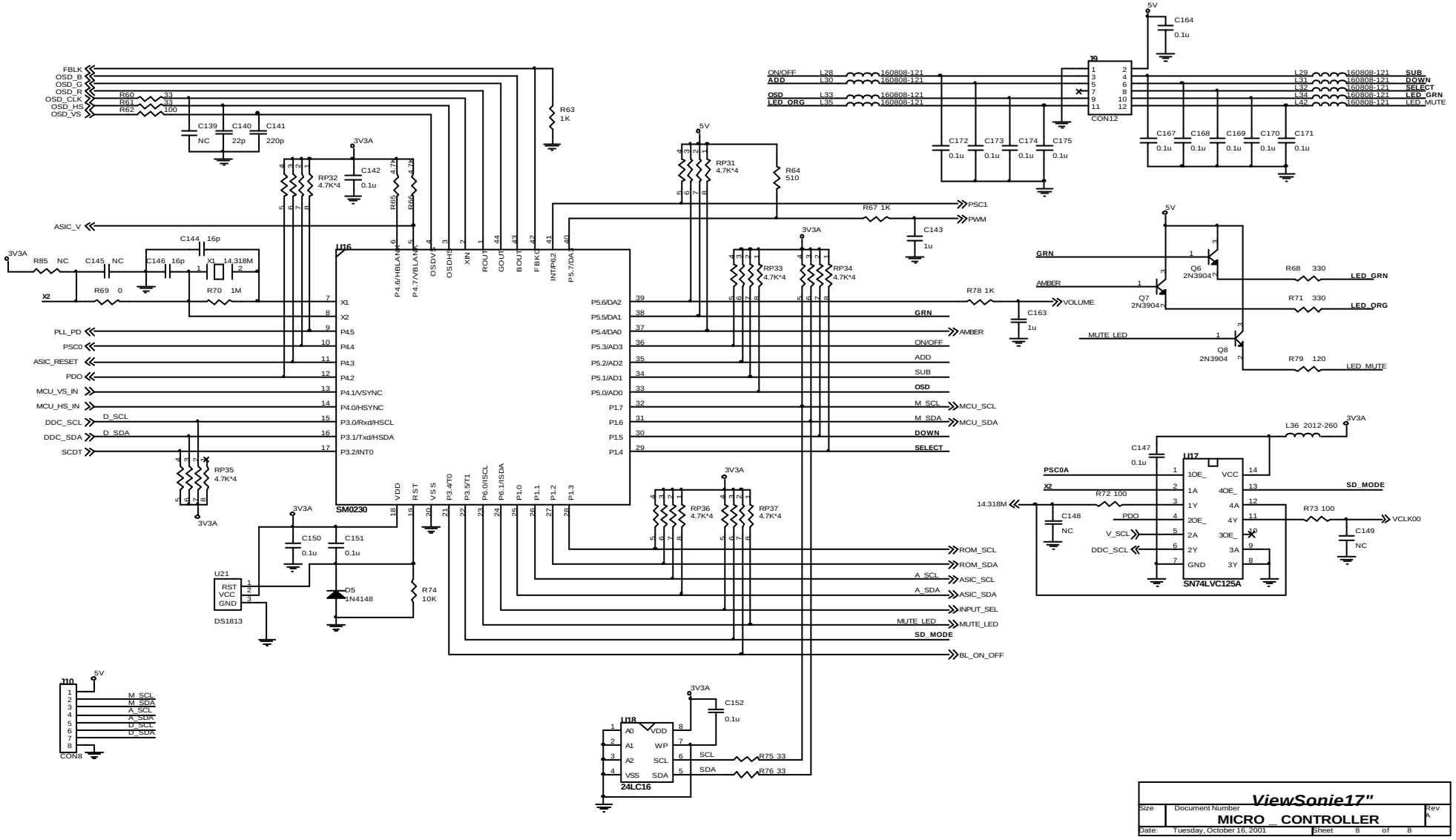






	ViewSonic17"	
Size	Document Number TTL	Rev A
Date: Tuesday, October 16, 2001	Sheet 7 of 8	

9.8 MCU


U16
SM0230
U17
SN74LVC125A
U18
24LC16
U21
DS1813
J10
CON8
J9
CON12
ViewSonic17"
MICRO__CONTROLLER
Date: Tuesday, October 16, 2001
Sheet 8 of 8